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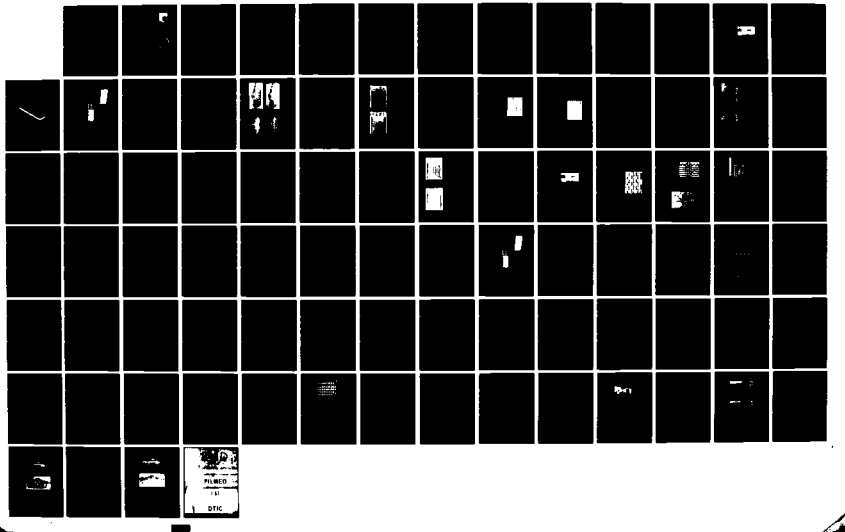

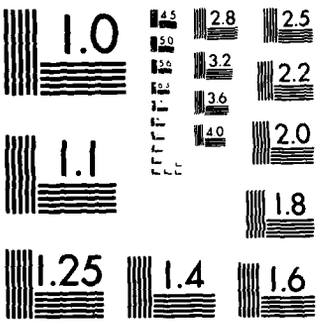

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PHASE II PROGRAMMABLE IMAGE PROCESSING ELEMENT (PIPE)

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October 1982

Final Report for Period 15 December 1980—15 June 1982

Approved for public release; distribution unlimited.

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Neigbornood Operators
Image Processing Brassboard

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The objective of this 18-month exploratory development effort was the fabrication and testing of the Programmable Image Processing Element (PIPE) LSIC developed under the Phase I contract and the design and fabrication of a brassboard to demonstrate the versality of the PIPE LSIC.

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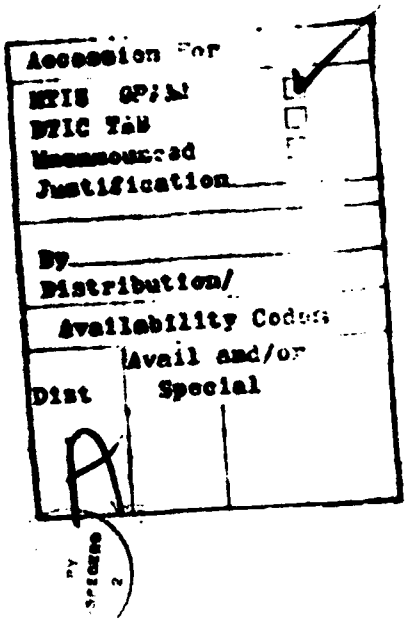
Two phases of IC processing were required because minor layout errors were discovered in the first-pass ICs, and the redesign, photomask generation, processing, and testing steps were repeated. The second-pass ICs were 100-percent functional and packaged in 64-pin dual in-line packages (DIPs) for use in the brassboard.

A flexible brassboard operating in or near real-time was developed to demonstrate the PIPE LSIC. Although simple, the brassboard operates the PIPE LSIC in both its serial and parallel modes and demonstrates its processing of vector/transforms and neighborhood operators.

Images composed of 512 by 512 8-bit pixels are formed in a frame buffer and processed at frame rates determined by the PIPE LSIC throughput, buffer memory speed, brassboard architecture, and the algorithm being computed.

Eight PIPE LSICs are used in the brassboard. For the 3 × 3 differential edge detectors, four PIPE LSICs calculate the horizontal response while the other four PIPE LSICs calculate the vertical response.



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SECTION I
INTRODUCTION

A. OVERVIEW

The advance of large-scale integrated circuit (LSIC) technology has spawned many new technologies and made many others economically feasible. Military signal-processing functions found in such applications as forward-looking infrared (FLIR) radar, guidance and control, and electronic countermeasure (ECM) systems have been significantly impacted. In particular, image-processing systems for video bandwidth reduction; FLIR automatic cueing; target detection, classification, and tracking; and image understanding must apply LSIC technology to be affordable in system constraints such as size, weight, power dissipation, cost, and reliability. Integrated circuits developed for such applications are most affordable when they can be used on several different programs. Such robustness can be accomplished by flexible, programmable designs or by functional designs that efficiently implement commonly used functions in a manner that allows them to be parameterized for each application.

The Programmable Image Processing Element (PIPE) is an example of a parameterized functional design. It implements the sum-of-products operator common to many image processing problems:

$$Y = \sum_{i=0}^{I-1} W_i X_i$$

where the term W_i represents a set of fixed, programmable weighting coefficients and X_i represents a set (or I-point sequence) of input samples. More specifically, if $I = 9$, this equation can implement the 3- by 3-pixel window operator used in image processing for high- and low-pass filtering, edge enhancement, and edge crispening. This same function can be used to calculate the coefficient of transforms such as Fourier, cosine, Hadamard, and Harr used in image and signal processing. It is also applicable in other signal-processing areas such as recursive and nonrecursive digital filtering.

Under Contract F33615-80-C-1180, the key to program success was the use of distributed arithmetic techniques to implement the sum-of-products operator without using digital multipliers, which could significantly impact image-processing systems.

B. OBJECTIVE

This contract represents the second phase of a previous contract (F33615-79-C-1763). The PIPE Phase I contract addressed only the design and photomask fabrication of the PIPE LSIC. The Phase II emphasis was on fabrication and testing of the PIPE LSIC developed under Phase I and the design and fabrication of a brassboard to demonstrate the versatility of the PIPE LSIC. There were three major efforts:

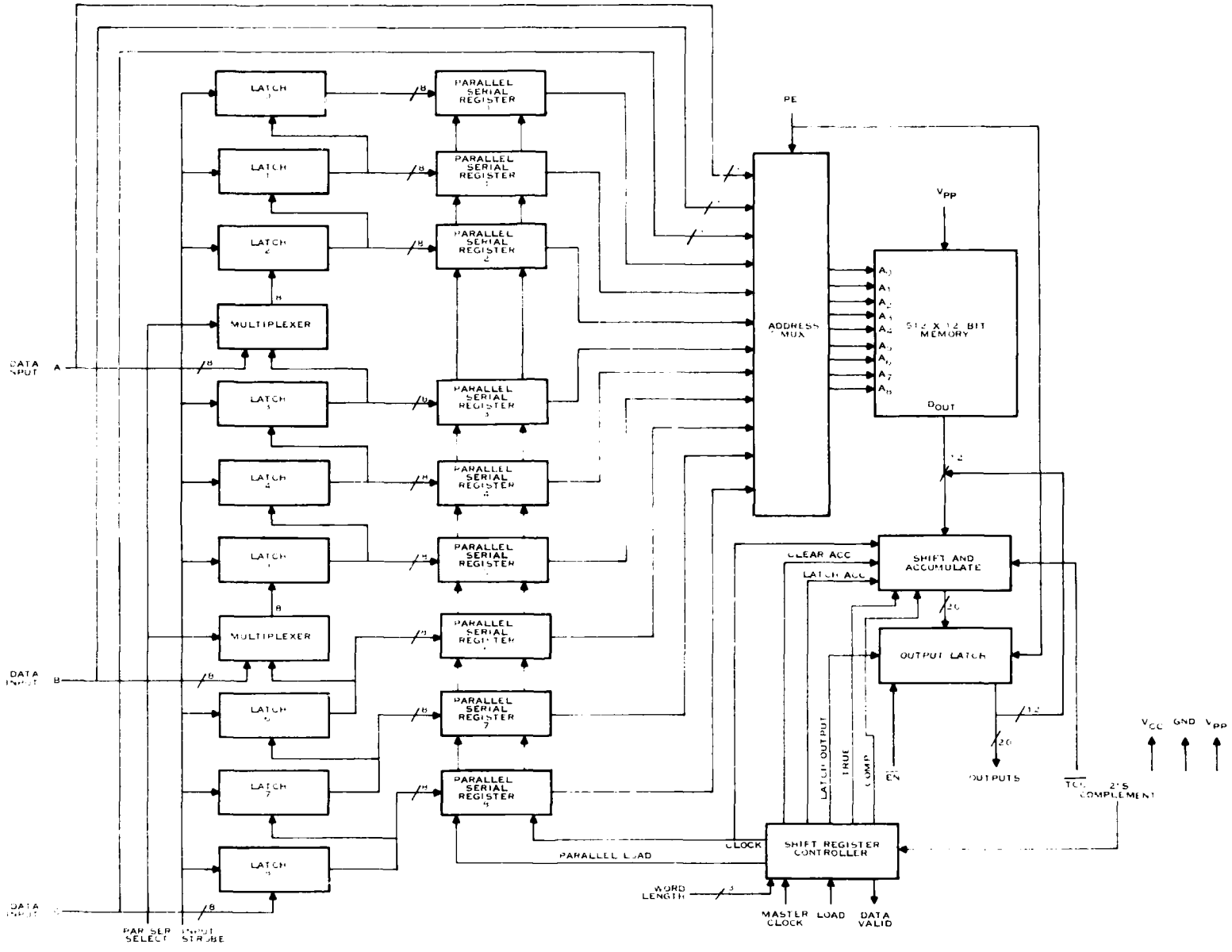


Figure 1. PIPE Architecture

PIPE LSIC development, the objective of which was to fabricate the PIPE LSICs using the photomasks generated in Phase I and perform functional evaluation. If any device errors were discovered, design, photomask generation, processing, and testing were to be repeated.

Brassboard demonstration system, with which to demonstrate the ability of the PIPE LSIC to implement image-processing algorithms on real-time video data.

Brassboard demonstration at AFWAL to provide a complete exchange of technical information regarding the PIPE LSICs and brassboard.

C. SUMMARY

Texas Instruments has successfully completed all of the objectives of the PIPE Phase II contract.

1. PIPE LSIC Development

Figure 1 is a block diagram of the PIPE LSIC. The input data A, B, and C are parallel words that can be loaded into input latches either serially or in parallel. Users control the mode of operation via the parallel/serial select control line, allowing the PIPE LSIC to operate on either 9×1 or 3×3 blocks of data. In the serial mode, all data are loaded through the C input pins and sequentially clocked into the latches in nine sample periods. In the parallel mode, data are loaded through the A, B, and C input pins into three separate input latches and then sequentially clocked into the other latches; thus, three sample periods are required to load all the input latches.

Bit-parallel words in the input latches are converted into bit-serial words by the parallel-to-serial registers; outputs of these registers form the 9-bit memory address. Shift-and-accumulate operations at the memory outputs complete the sum of products. Users can designate either signed or unsigned arithmetic for these operations.

Tristate output latches are provided for off-chip buffering. All timing and control for the parallel-to-serial registers, the memory, shift-and-accumulate, and the output buffers are generated on the chip using a simple shift-register controller.

Full 8-bit input and 20-bit output operations of the PIPE require 59 pins (Table 1). This can be reduced to 40 pins if 6-bit input data and only 8 bits of the output are used. The pins required for word-length selection, input type (parallel or serial), and data format (2's complement or magnitude) can be eliminated by on-chip bonding to the V_{DD} or ground pin for fixed applications.

Figure 2 is a photomicrograph of the PIPE LSIC. The LSIC is implemented in N-channel metal oxide semiconductor (NMOS) technology using conservative 5-μm design rules. An erasable, programmable ROM is used to implement the memory function of the ROM-accumulate algorithm. Total bar size is approximately 43 mm^2 (240 $\times$ 270 mils^2).

IC processing required two passes because some minor layout errors were discovered in the fast-pass ICs (the shift register controller, clock driver, and tristate output latches), which prevented them from being completely functional but did not prevent detailed evaluation of the remaining circuits. The redesign, photomask generation, processing, and testing steps were repeated.

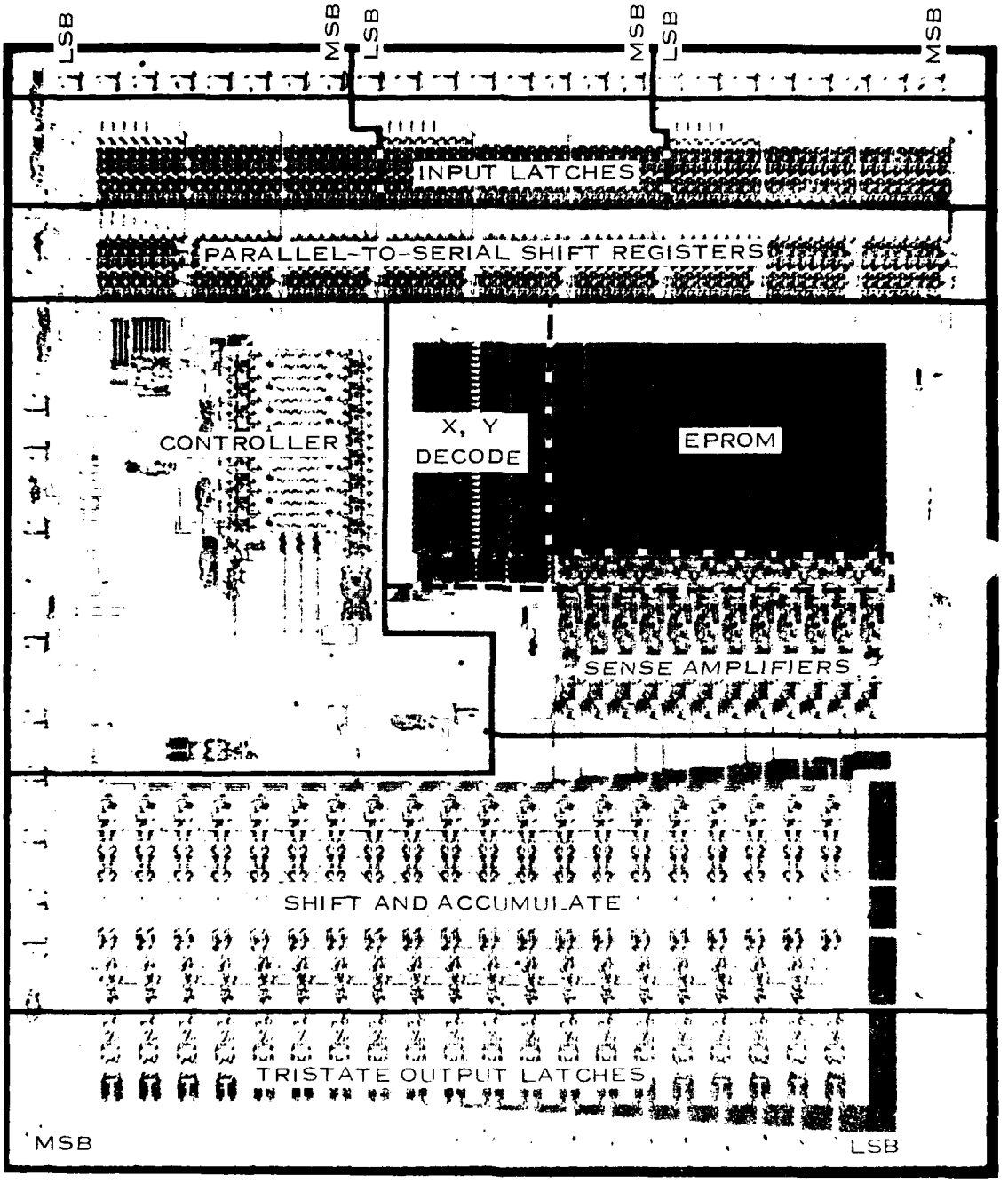


Figure 2. Programmable Image Processing Element (PIPE)

TABLE 1. PIPE LSIC INPUT/OUTPUT PIN REQUIREMENTS

Control Line(s)	No. Pins	Function
Data-A input	8	Input data
Data-B input	8	Input data
Data-C input	8	Input data
Parallel/serial select	1	Determines modes of chip operation (3 × 3 or 9 × 1 operations)
Input strobe	1	Indicates valid input data and latches data into input latches
Word length (BCD code)	3	Defines word length of input data
Master clock	1	Square-wave clock provided for system timing
Load	1	Initiates parallel-to-serial data conversion
Data valid	1	Output signal indicating complete calculation
Enable (EN)	1	Used to tristate or enable output bus
Data too fast	1	Inhibits input srobe during parallel load operations
Outputs	20	Output data
2's complement coefficients (TCC)	1	Used to set sign bit of output word
2's complement data (TCD)	1	Defines signed or unsigned magnitude data operation
V_{DD}	1	Single +5 V operating supply
V_{PP}	1	Normally at +5 V, but taken to +25 V for EPROM programming
G_{ND}	1	Substrate bias
Total	59	

During the redesign phase, an automated schematic verification of the PIPE LSIC was perfc med. This verification compared the actual LSIC layout with the circuit schematic and, with the exception of some minor device size deviations in the TTL-to-MOS clock driver and the NOR buffers in the input controller section, nc layout errors were discovered. After the schematic verification, new photomasks were generated (7 of the 12 photomasks were replaced) and second-pass PIPE LSICs were processed and evaluated. The second-pass ICs were 100-percent functional.

Figure 3 shows a PIPE LSIC packaged in a 64-pin dual in-line package (DIP). The operating characteristics of the PIPE LSIC are listed in Table 2.

2. Demonstration Brassboard

To demonstrate the PIPE LSIC, a flexible, completely self-contained brassboard (Figure 4) operating in or near real-time was developed. It is 17.0 × 18.5 × 9.0 inches, weighs 46 pounds, and dissipates 87 W. Although simple, the brassboard operates the PIPE LSIC in both its serial and parallel modes and demonstrates its processing of vector/transforms and neighborhood operators. The brassboard accepts

TABLE 2. PIPE CHARACTERISTICS

	Maximum	*Minimum*
Maximum operating voltage	10 V	4.5 V
Maximum programming voltage	35 V	17 V
Maximum strobe frequency	12 MHz	–
Maximum clock frequency*	12 MHz	1 kHz
Typical EPROM access time	170 ns	–
Power requirements	800 mW at 5 V	–
Memory erase time (2537 Å at 15 W-s cm^{-2})	–	40 min.

*Dependent on EPROM access time and mode of operation.

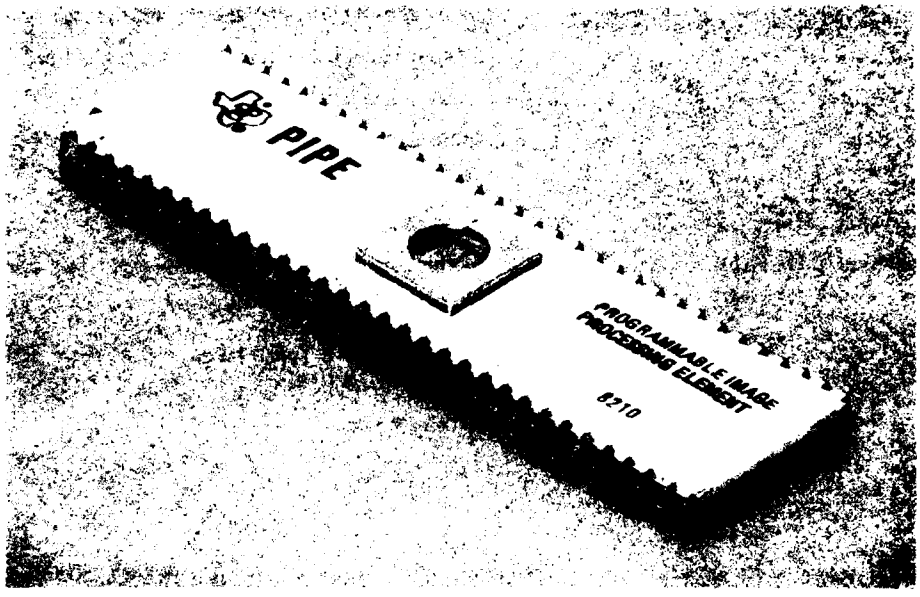


Figure 3. *PIPE LSIC*

single-line video as input and displays processed results on a standard TV monitor for evaluation. It is constructed of 13 wire-wrapped boards, each capable of containing 50 to 60 integrated circuits in 16-pin DIPs; a one-to-one correspondence exists between these boards and the blocks shown in Figure 4. The analog-to-digital converter (ADC) digitizes the incoming video to 8 bits for further digital processing.

Images composed of 512 by 512 8-bit pixels are formed in a frame buffer and processed at frame rates determined by the PIPE LSIC throughput, buffer memory speed, brassboard architecture, and the algorithm being computed. Pixel processing rates for the PIPE LSIC are limited by the EPROM access time.

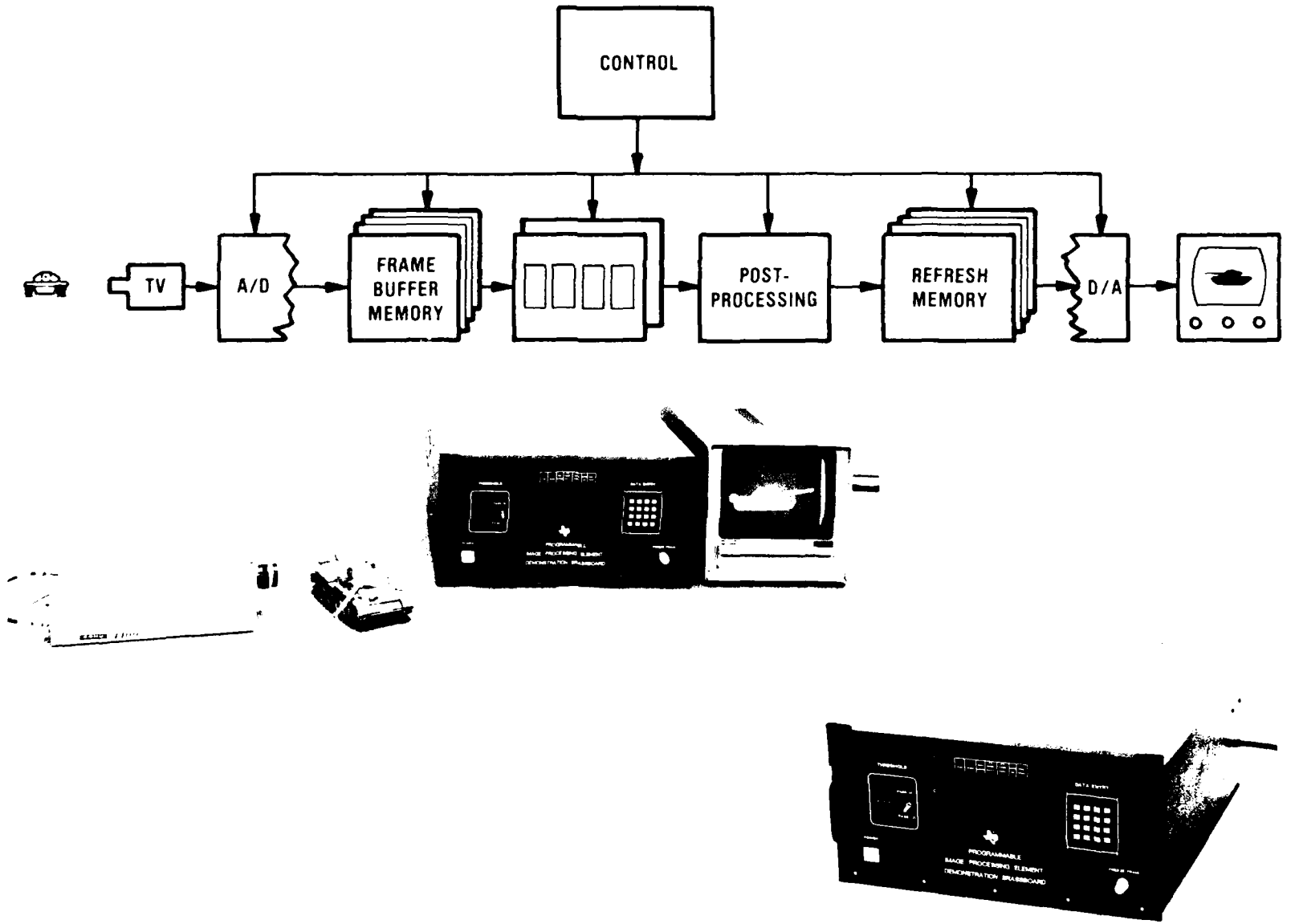


Figure 4. PIPE Demonstration Brassboard

Eight PIPE LSICs are used in the brassboard. For the 3 × 3 differential edge detectors, four PIPE LSICs calculate the horizontal response while the other four PIPE LSIC's calculate the vertical response. The template-matching edge detectors also require eight PIPE LSIC's for maximum throughput, with one template assigned to each PIPE. The output of the PIPE LSIC's is processed according to the operation selected (e.g., calculate the magnitude and orientation for the differential edge detectors or find the maximum response for template-matching edge detectors). A minimum amount of interface between the user and the PIPE LSIC is required to communicate the type of operations to be performed, the format of input data, etc. This interface is implemented through a control panel for the demonstration brassboard. This control panel uses a 16-key calculator-style keyboard for command entry, a 24-character alphanumeric LCD for displaying current operating parameters and for prompting the user for new parameters, and a 3-digit thumbwheel switch for entering threshold levels. The user commands the brassboard to perform various operations by responding to seven prompts with seven single keystroke replies. These prompts query the user for operating parameters such as parallel or serial input, 2's complement data, 2's complement weighting coefficients, word length, weighting arrangement (i.e., do all eight LSICs contain the same weights?), postprocessing operation (magnitude, maximum, or no operation), and sliding or nonsliding operation.

A display-refresh memory and digital-to-analog converter (DAC) provide analog data in a standard television-monitor format. Both the ADC and DAC are high-speed (10-MHz), 8-bit, commercially available components.

Eight boards implement the frame buffer and refresh memories: four identical boards implement the frame buffer memory, and four identical boards implement the refresh memory. The buffer and refresh memory boards are essentially identical, differing only slightly in the write and output sections. Both memories store a complete video frame ($512 \times 512 \times 8$) and are designed with $16K \times 1$ dynamic random-access memories (RAMs). Each board holds two bit planes, i.e., $512 \times 512 \times 2$ bits. The frame buffer memory is designed to provide vertically related pixels from three adjacent lines simultaneously as inputs to the PIPE LSICs for parallel mode operation. Data are available also in serial format from a single port for serial-mode operations. Although this memory captures data from the ADC at a 10-MHz rate (100 ns/pixel), a special demultiplexing scheme permits use of memories with slower access times. The refresh memory has two functions: accept data from the postprocessing electronics and provide digital words to the DAC for reproducing analog video. These functions cannot be performed at the same speed but are synchronized. Each memory cycle is designed to read and provide time for a possible write if data are available from the postprocessing electronics.

An LSIC input controller and LSIC output controller control the eight PIPE LSICs in the demonstration brassboard. The input controller uses the input strobe pulse and a BCD value of the number of input strobes between the parallel-to-serial conversions to generate a load pulse for the PIPE LSIC shift-register controller. Corresponding inputs of the eight PIPE LSICs are connected. A counter generates a

load pulse to each LSIC after the correct number of input strobes. Thus, the devices can be loaded in parallel or sequentially in various combinations. For differential edge detectors, the first four PIPE LSICs calculate the horizontal response while the last four PIPE LSICs calculate the vertical response; therefore, the first and fifth PIPE LSICs need the same data, the second and sixth PIPE LSICs need the same data, etc. For calculating transform coefficients and template-matching edge detectors, all eight PIPE LSICs must be loaded with the same data, i.e., have the same load pulse.

The outputs of the eight PIPE LSICs are controlled by the LSIC output controller that selects any one, any pair, or all the outputs for postprocessing. The DATA VALID output of the PIPE LSIC multiplexes the outputs of the eight PIPE LSICs in much the same way that the load pulse demultiplexed the inputs; thus, their outputs can be loaded into latches either sequentially or in pairs. For operations in which the outputs are valid simultaneously, the LSIC output controller multiplexes the outputs into one latch.

A limited amount of postprocessing electronics is provided on the demonstration brassboard to combine outputs of the PIPE LSICs. To complete the magnitude and orientation calculation of the differential edge operators, the ability to sum the absolute values and calculate a 3-bit approximation to the direction vector is provided. The ability to find the maximum of eight inputs is provided for determining edge orientation using the template-matching edge detectors. A variable threshold permits evaluation of the various edge detectors. Also, for some types of operations, postprocessing is not required; therefore, an option to bypass the postprocessing function is provided.

The results of using the PIPE demonstration brassboard to implement a 3×3 low-pass filter, a Sobel differential detector, and a 5-level template-match edge detector appear in Figure 5. The technical aspects of the PIPE LSIC development, the demonstration brassboard system, and experimental results are discussed in Section II, and a more detailed discussion of the PIPE LSIC design and operational characteristics can be found in the Phase I final report.*

*T.F. Cheek, W.L. Eversole, and J.F. Salzman, "Programmable Image Processing Element," Final Report, Contract No. F33615-79-C-1763 (November 1980).

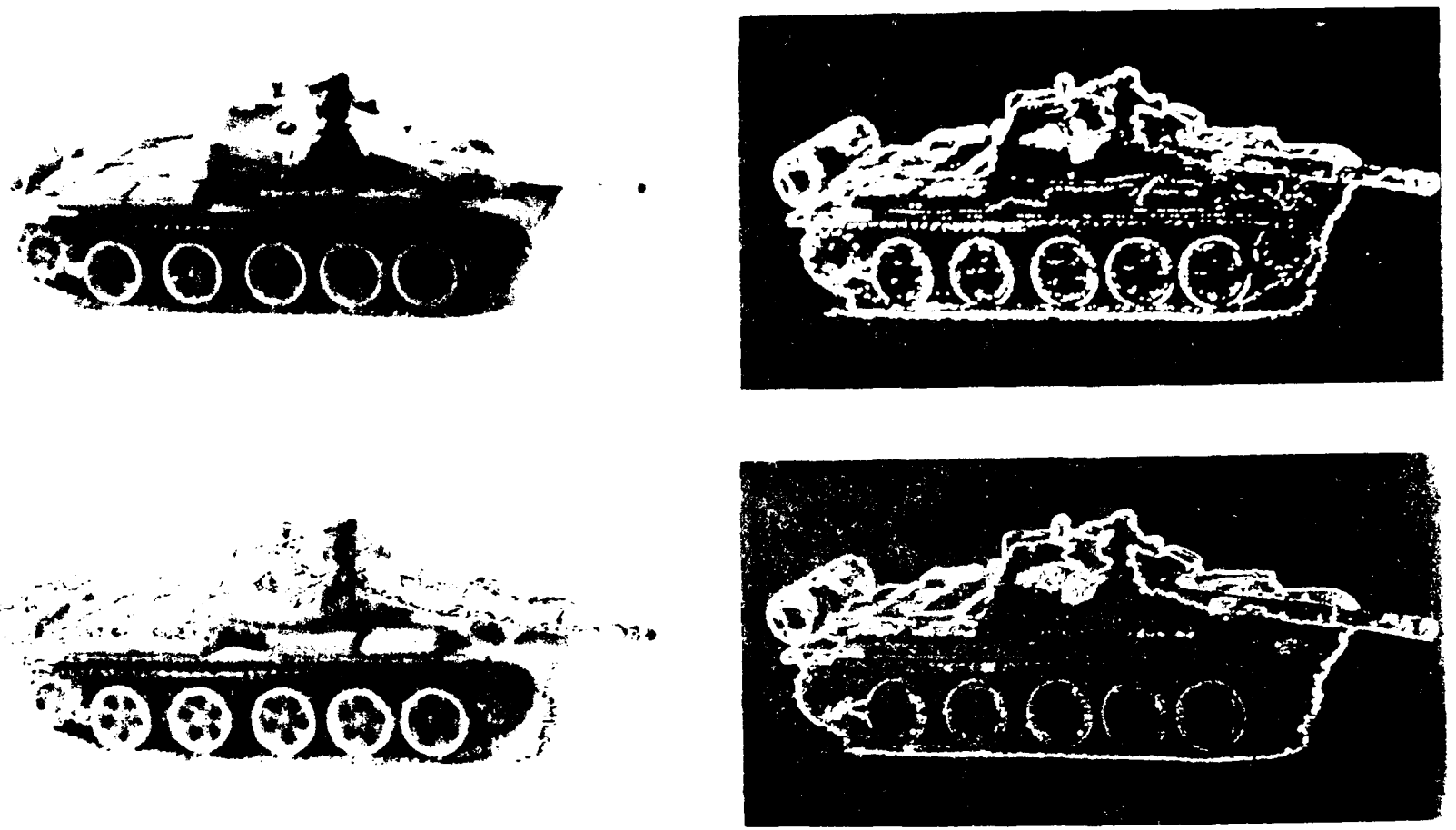


Figure 5. Operation of PIPE Demonstration Brassboard

SECTION II
TECHNICAL DISCUSSION

Texas Instruments has fabricated and evaluated a programmable image processing element (PIPE) large-scale integrated circuit (LSIC) and, to demonstrate it, has developed a flexible brassboard capable of operating in real-time. Details of the PIPE LSIC development and the design of the demonstration brassboard are discussed in this section.

A. PIPE LSIC DEVELOPMENT

The objective of the PIPE LSIC development was to fabricate the PIPE LSICs using the photomasks generated in Phase I (Contract F33615-79-C-1763) and perform functional evaluation. To correct any device errors found during initial testing, time in the Phase II schedule was included for redesign, photomask generation, and testing.

1. Phase II First-Pass Results

During Phase II, PIPE LSICs were processed using photomasks produced during Phase I PIPE development. The PIPE LSICs were processed in DMOS II (Dallas MOS Front End No. 2) using the standard 25XX, 5-μm EPROM process. In January 1981, 20 slices were started through the process flow; on 27 February 1981, 17 were finished. Three slices were damaged in the process flow.

The PIPE LSICs were probed to determine the quality of the processing. The processing parameters closely corresponded to the design models. Figure 6 shows the characteristics of a typical enhancement and depletion transistor. The designed threshold (V_T) was 0.8 V and -3.0 V, respectively.

Circuit probing then started utilizing a low-capacitance probe, which is required in NMOS circuit probing owing to loading effects and drive limitations. Figure 7 is a schematic of the FET probe that was used on the various LSIC circuits.

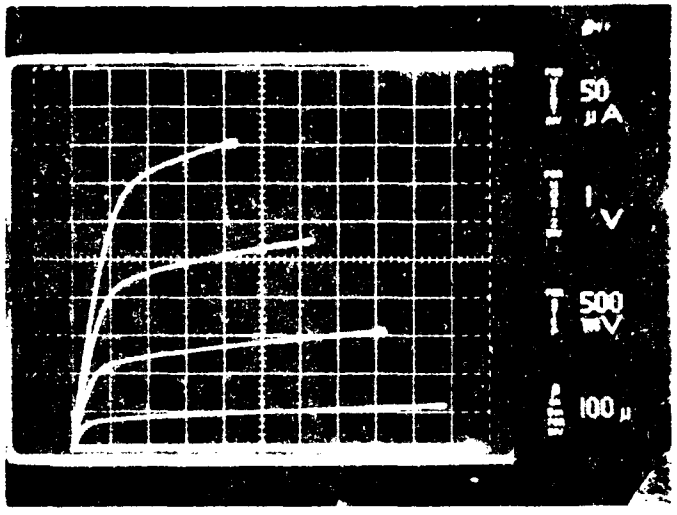
Initial circuit probing indicated circuit errors. Checking the Calcomp plots against the schematic on the suspected areas revealed minor layout errors.

Parallel efforts involving slice-level testing were temporarily halted after the initial probe testing showed circuit errors. While these errors prevented the LSIC from being completely functional, they did not prevent detailed evaluation of the remaining circuits in the redesign. Table 3 lists the inoperative circuits and reasons for their failure, and the following subsection discusses them as well as the various redesign modifications in more detail.

2. Circuit Evaluation and Redesign

The most common building block used on the PIPE LSIC is the MOS latch, so the input latch structure was the first circuit evaluated.

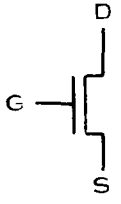
Figure 8 is a block diagram schematic and oscilloscope photograph of a functional PIPE LSIC latch. The input is TTL level (approximately 2.4 V), and the latched output is MOS level (approximately 5 V). Both the nine 8-bit input latches and the parallel-to-serial shift registers use this standard MOS latch.

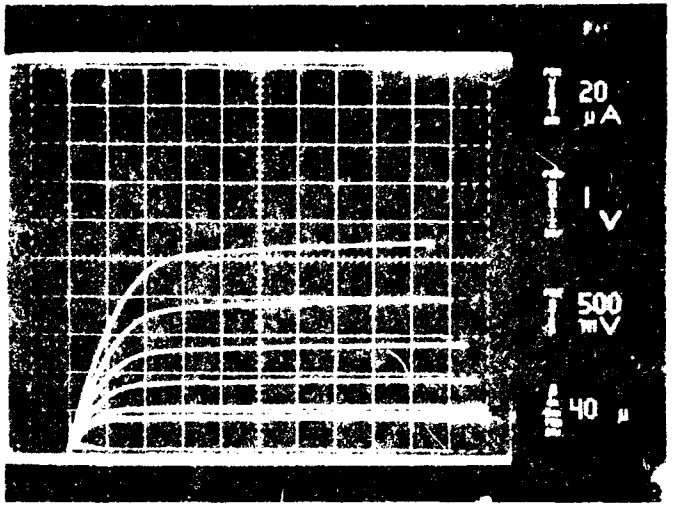


ENHANCEMENT
TRANSISTOR

V_T = 1.0V

W/L = 1.0/0.2





DEPLETION
TRANSISTOR

V_T = 2.3V

W/L = 1.0/1.0

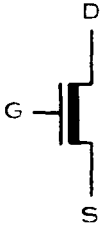


Figure 6. First-Pass PIPE LSIC Transistor Characteristics

TABLE 3. FIRST-PASS PIPE LSIC CIRCUIT ERRORS AND CAUSES

Inoperative Circuits	Failure Cause
Controller NOR buffers	Layout error
Clock driver	Layout error
Tristate output buffer	Layout error
Shift and accumulate	Design error
Controller	Design error

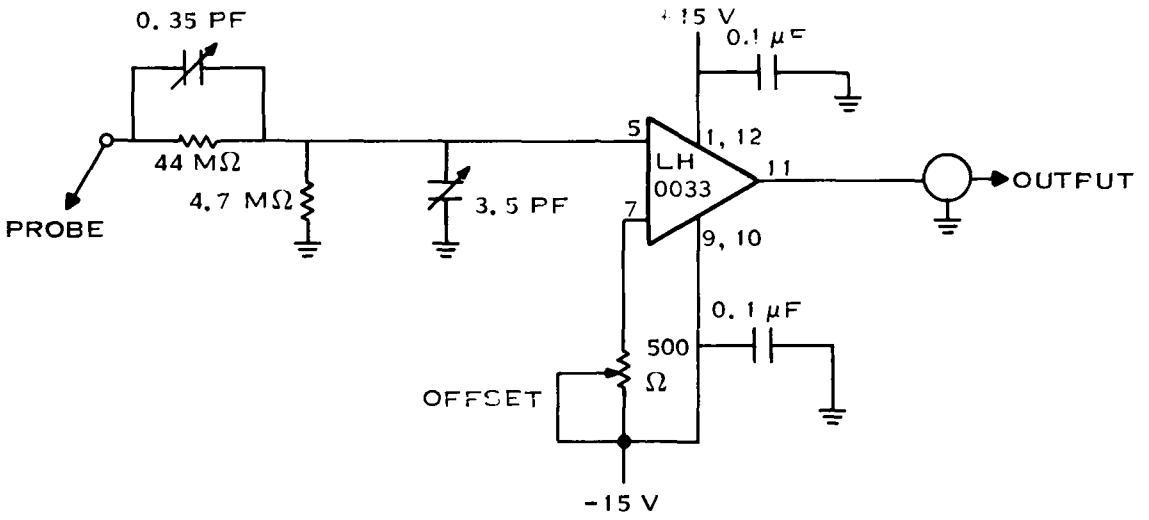
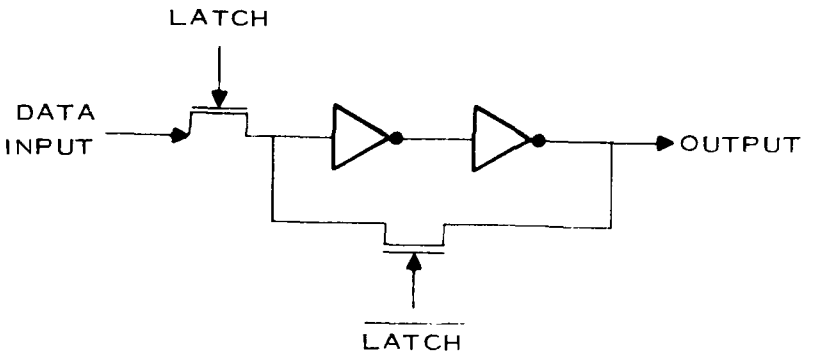


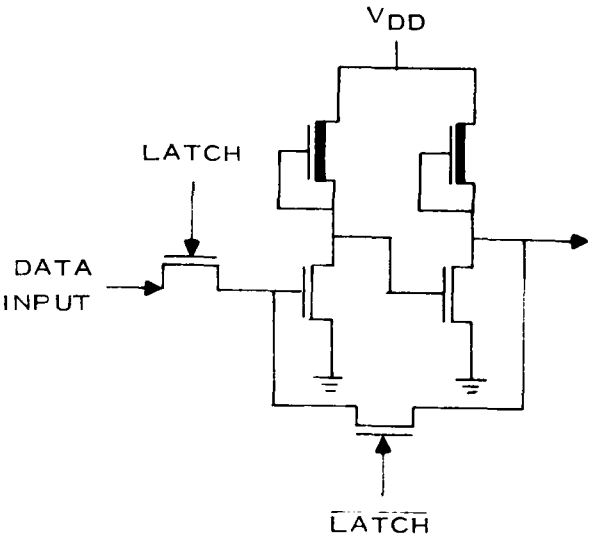
Figure 7. Low-Capacitance Active Probe Used in PIPE LSIC Evaluation

Figure 9 shows the operation of a parallel-to-serial shift register. The 8-bit data on the left was input to the serial port of the PIPE LSIC and strobed serially through the input latches and converted into bit serial form for addressing the EPROM. This demonstrated the functionality of the input section (input latches, multiplexers, and parallel-to-serial shift registers). However, circuit evaluation of a possible design problem appeared. Critical timing between the strobe and load pulse indicated that, if a strobe occurred during the parallel load, data transfer into the parallel-to-serial shift registers could be incorrect. To prevent a strobe during the data transfer operation, a strobe inhibit circuit [referred to as data too fast (DTF) circuit] was added. The implemented logic function used for the DTF circuit is shown in Figure 10. When the DTF control line is low, the parallel load pulse is passed to NOR2 and is NORed with the STROBE pulse. When DTF is high, the STROBE circuitry is unaffected by the load pulse.

The next section to be evaluated, the PIPE LSIC 512 × 512 bit EPROM, was found to be fully functional.



LATCH BLOCK DIAGRAM



LATCH SCHEMATIC DIAGRAM

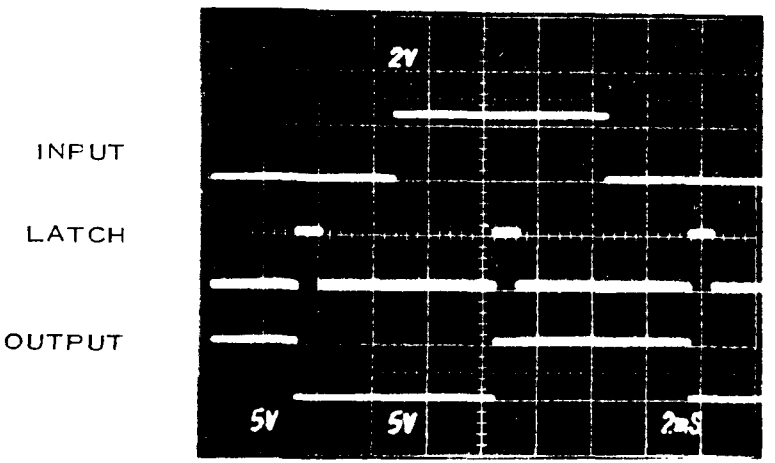
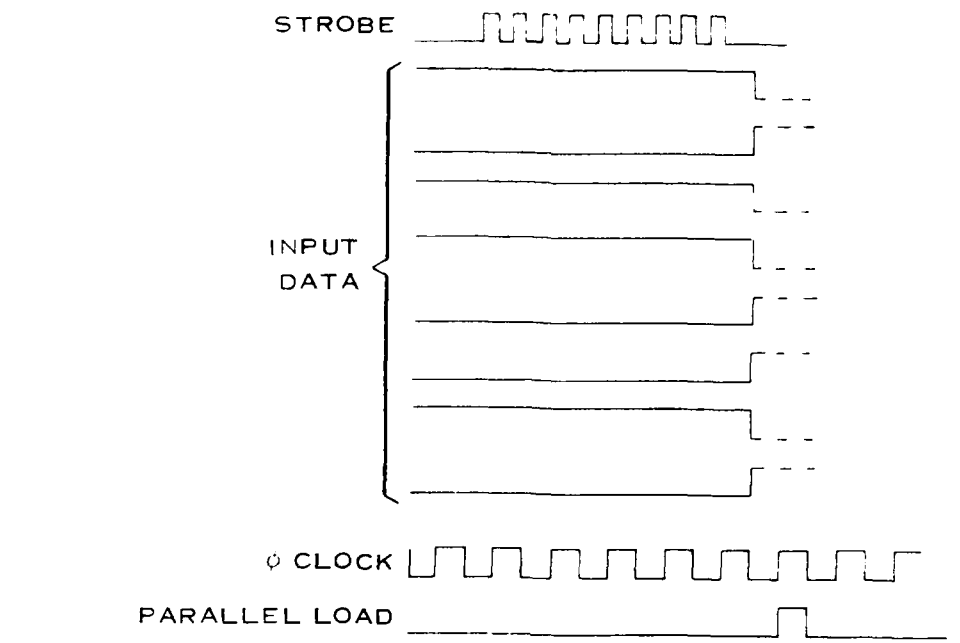


Figure 8. NMOS Latch Circuit



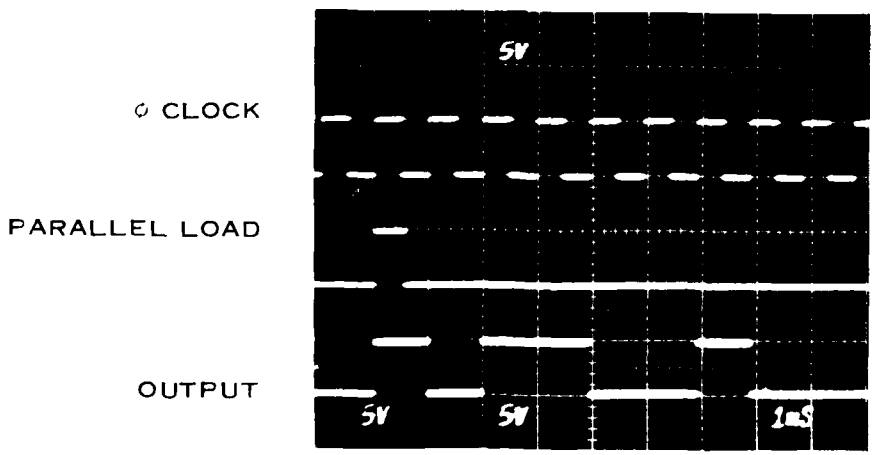


Figure 9. Input Latch/Multiplexer – Parallel/Serial Shift Register Operation

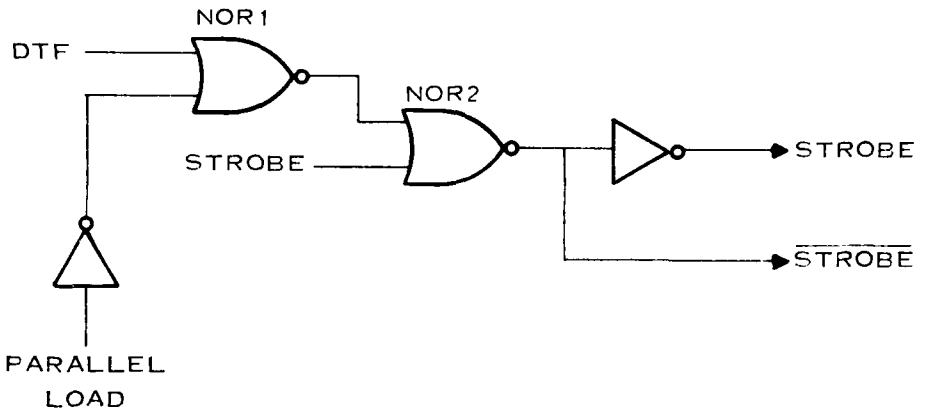


Figure 10. PIPE LSIC Strobe Inhibit Circuit

Before programming, the EPROM was erased by exposing the IC to a high-density ultraviolet light (wavelength of 2537 Å). (After erasure, all bits are in a logic high state and logic lows are programmed into the desired locations.) The EPROM was programmed by raising the programming voltage, V_{pp}, to +25 V for 50 ms. (By raising V_{pp}, the address multiplexer is forced to select the three MSBs from each of the three input words A, B, and C to form the 9-bit address to the EPROM.) Data to be programmed was applied to the tri-state buffer bond pads. The addresses and data were changed and the programming process repeated several times.

Data was read from the EPROM by enabling the program control line (logic level 1) via a special bond wire connection, thus providing a direct path for the memory address lines at all times. Data was read from the internal 2 × 2 mil^2 test pads at the output of the memory preceding the shift-and-accumulate circuitry. These pads were removed during redesign in an attempt to improve memory performance.

Utilizing a special low-capacitance probe, access times were measured at two widely separated bit locations of the EPROM, as shown in Figure 11. (Access times are dependent on bit location in the EPROM because of capacitive loading of the address and bit select lines.) Figure 12 shows access times measured at two locations. The bit location with the shortest address and bit select lines had an access time of 100 ns, while the location farthest from the address buffers had the longest address and bit select lines, resulting in access time of 180 ns. Another important parameter affecting access time is the threshold of the EPROM's floating gate storage transistors. Although the measured thresholds were within the acceptable range for operation, they were slightly high, resulting in slower access times.

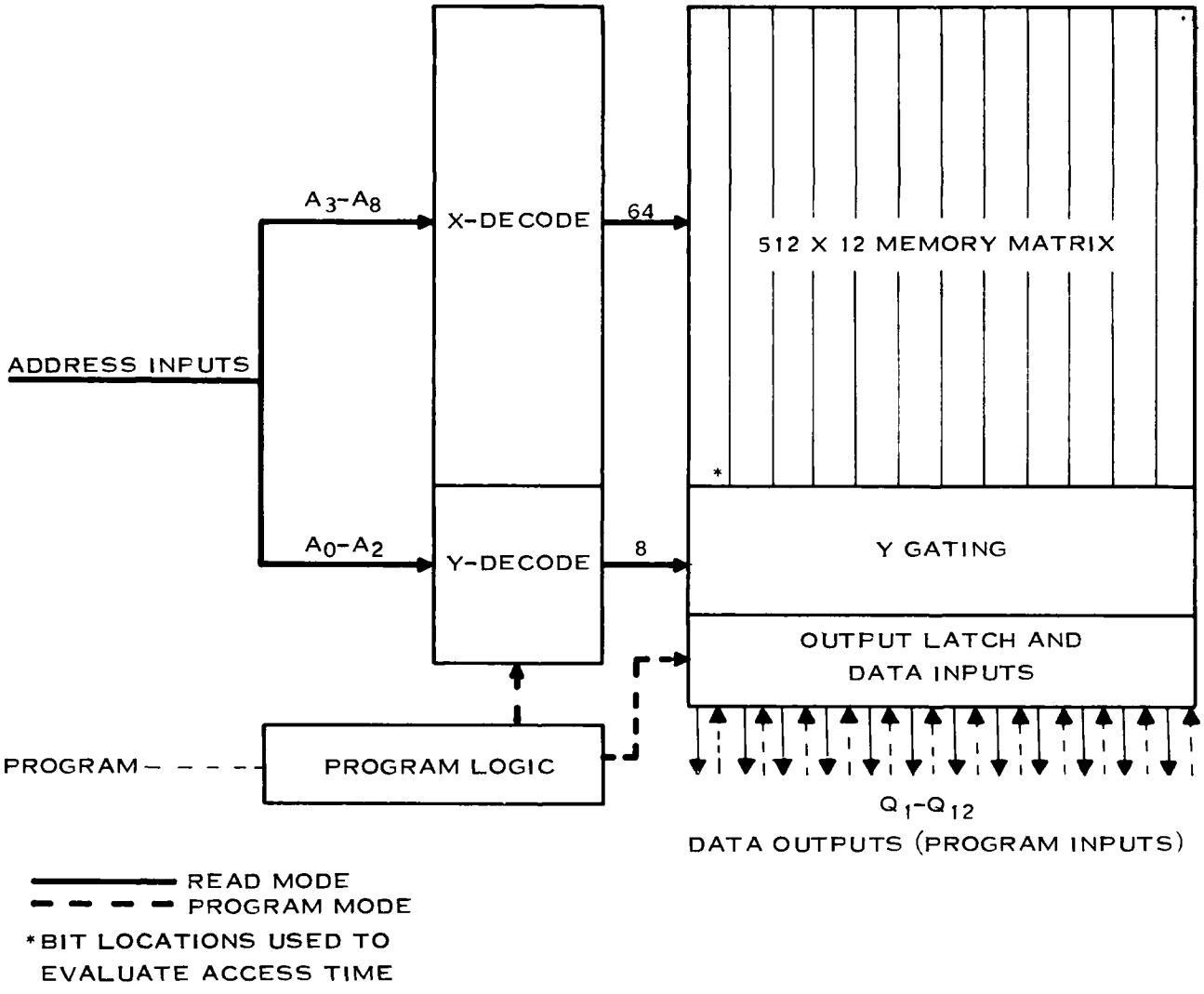
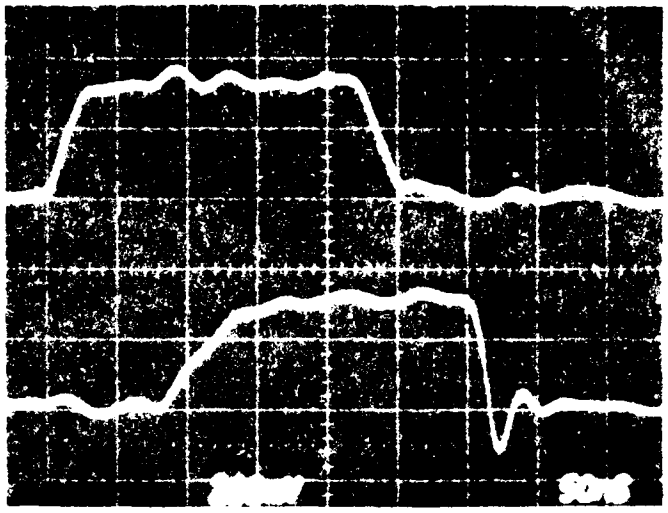
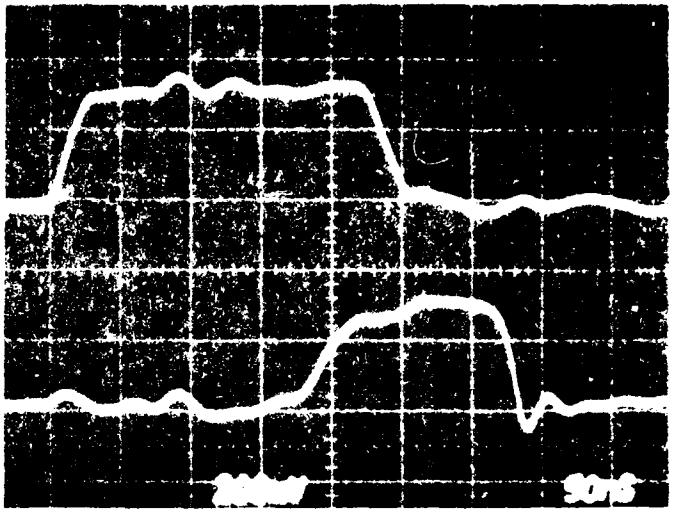


Figure 11. PIPE 512 × 512 EPROM Memory Configuration



ADDRESS INPUT

DATA OUTPUT



SHORTEST ADDRESS AND BIT SELECT LINES

100 NS ACCESS TIME

LONGEST ADDRESS AND BIT SELECT LINES

180 NS ACCESS TIME

Figure 12. PIPE EPROM Access Times

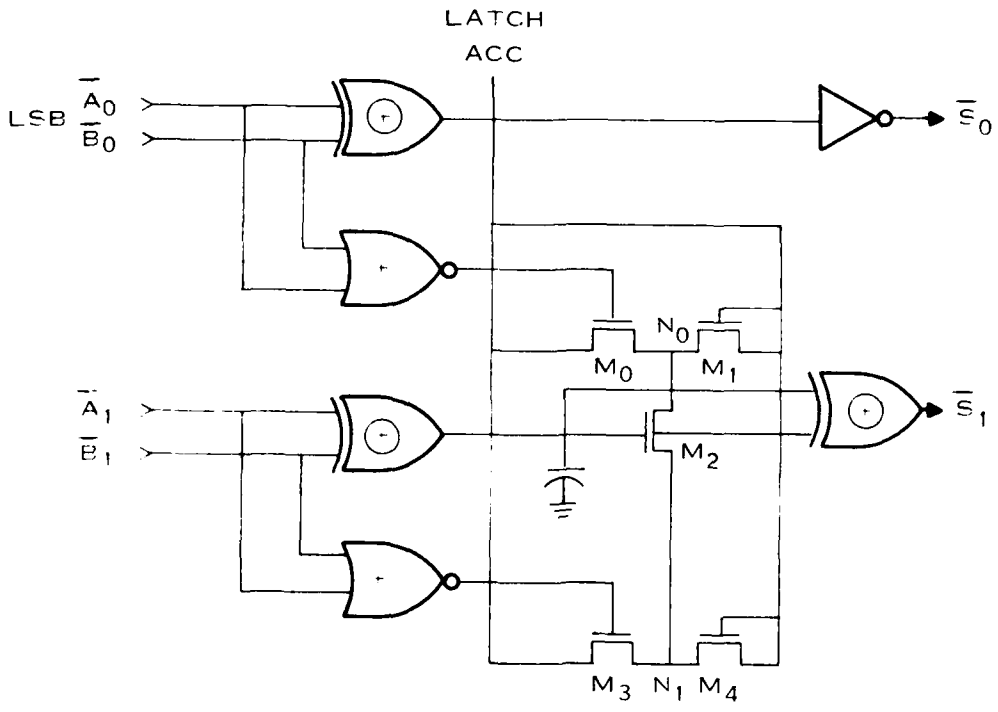


Figure 13. Two-Bit Dynamic Adder Used in PIPE LSIC Shift-and-Accumulate Circuitry

The access time was somewhat longer than expected, and lower transistor thresholds were sought on the second-pass processing. Another step to improve access time with minimal increase in power assumption was to increase the size of the transistors in the memory drivers from the parallel-to-serial shift register.

Next, the shift-and-accumulate circuitry was evaluated. The full adders and the carry-sum latches proved to be fully functional, but a design error was found in the dynamic adders. Figure 13 shows the 2-bit dynamic adder.

During shift-and-accumulate operation, a latch accumulate (LATCH CC) pulse precharges the capacitive nodes N_0 and N_1 to a logic high through transistors M_1 and M_4, respectively. However, because of transistor leakage, the two nodes discharged slightly when the LATCH CC pulse went low. A solution was easily derived: the drains of the precharge transistors were connected to the V_{DD} rail instead of the LATCH CC line; in this configuration, less current is supplied by the LATCH CC pulse and any leakage, as long as it is small, enhances the precharge node voltage. The new design, which proved itself in the second-pass results, is illustrated in Figure 14.

Next examined in detail was the shift register controller. Two layout errors were discovered. First, the TTL clock buffer and the NOR gate buffers had nodes that were incorrectly connected. Second, under certain power-up conditions during computer simulation, the output of latch SR_0 could have a logic 1

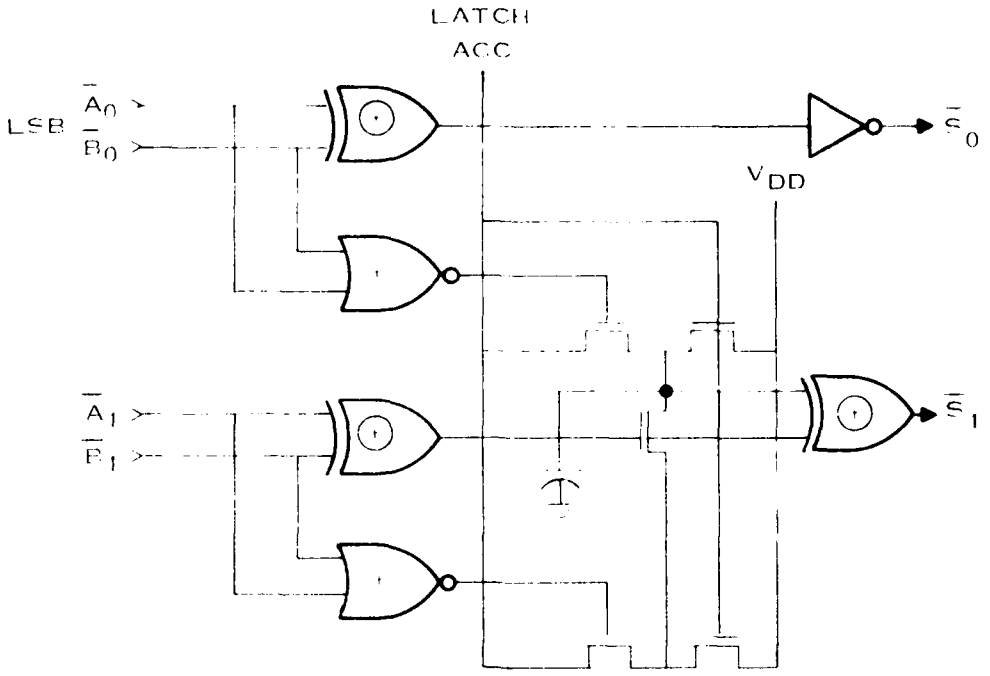


Figure 14. Two-Bit Dynamic Adder Design Change

while outputs of the data latches (D_0 through D_7) each have logic 0. This places a logic 1 on the clear input of data latch DL_{00}, producing a logic 0 on its output. The LOAD input line would become inoperative because of the logic 1 on the clear input latch DL_{00}, and the shift register controller would be in a stable, yet invalid, operating mode. To alleviate this potential problem, a power-on reset function was designed into the controller. Figure 15 is a partial diagram of the controller with the addition of the power reset function.

Next, layout errors in the tristate output buffer, NOR bus driver, and clock driver were corrected and a complete detailed computer simulation made on each section. It was discovered that not all stray capacitance was used in the initial simulations during Phase I and that this stray capacitance degraded the overall speed performance although a 10-MHz input data rate was still achievable. Design errors were corrected and computer simulation indicated operational circuits.

As indicated in Table 4, 7 masks of the original 12 were changed to correct defects.

3. Technology Used in Redesign

The front-end loading of DMOS II caused a slip in schedule for reprocessing the PIPE LSIC but also provided the time necessary to use a new design aid. The new tool is actually computer software, which replaces visual and manual plot checking. The program consists of two parts. The first routine checks the actual layout against predefined layout rules. For example, a metal line contacting a polysilicon line must-

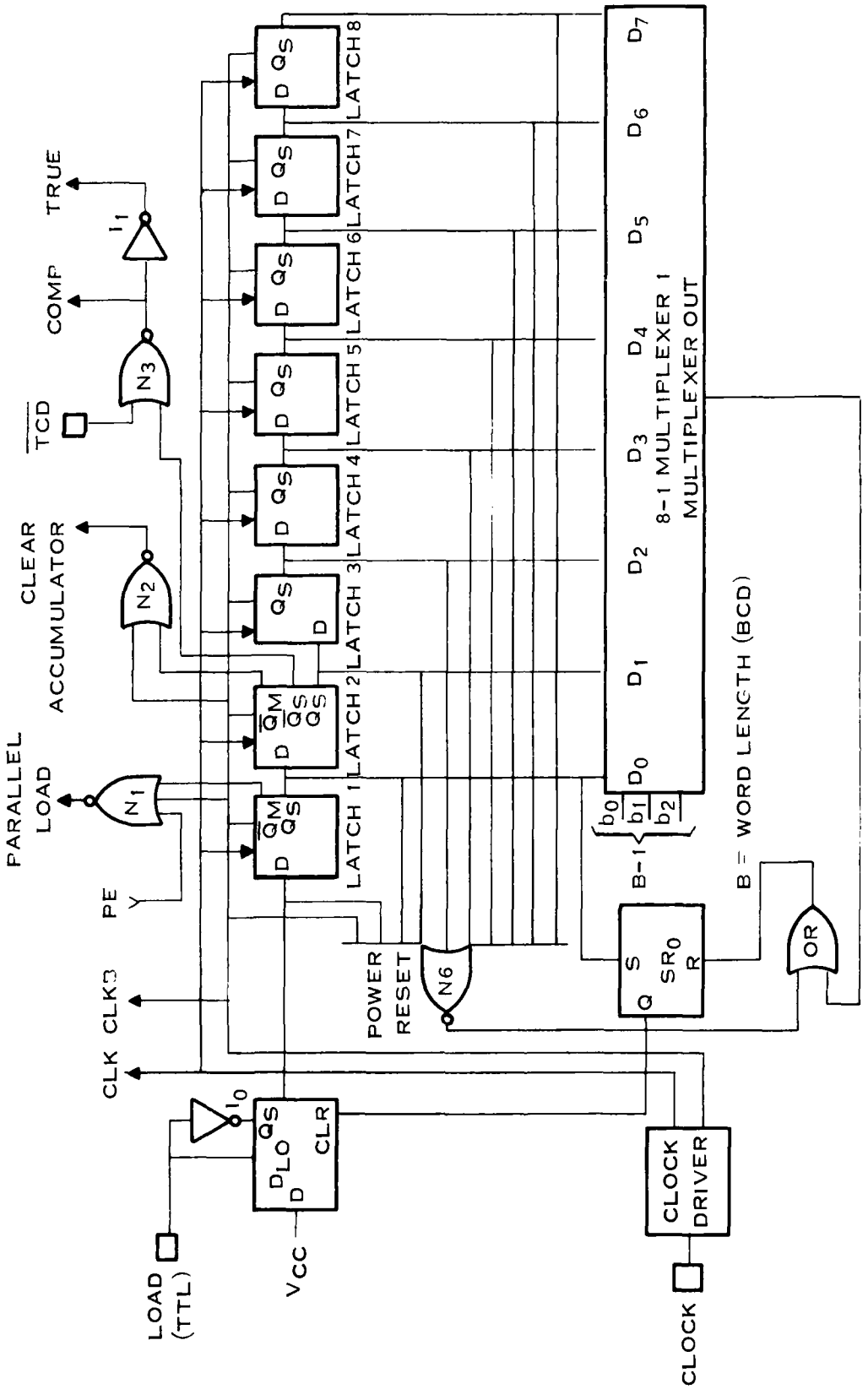


Figure 15. PIPE LSIC Controller With Reset

TABLE 4. PIPE MASK LEVELS

Mask No.	Level Name	Second-Pass Mask Changes
817–256	Inverse moat	*
817–257	Metal	*
817–258	Oxide removal	
817–259	N^- implant	
817–260	P^+ implant	
817–261	Depletion implant	*
817–262	Natural implant	
817–263	Contact 2, Coat 1	*
817–264	Contact 2, Coat 2	*
817–265	Polysilicon, Level 1	*
817–266	Polysilicon, Level 2	
817–267	Contact 2, Coat 3	*

meet certain guidelines. Figure 16 shows a simple example for the 5-μm technology used on the PIPE LSIC; this is a jumper where a signal is passed over another line. This requires a minimum of six rule checks on spacing and overlap, with each rule set defined by the particular technology used.

The second part of the verification involves the actual "circuit." Each circuit is described by its transistor and node connection makeup. This is referred to as the HDL description (hardware description language). Figure 17 shows an example of the TTL clock driver circuit and its HDL description.

A description similar to that shown in Figure 17 is then generated by software using the actual layout data. The two HDL descriptions are then compared for a match. If an error has occurred, a conflict message is generated and the user is notified of the error via computer printout. Figure 18 is an example of the verification routine and software flow.

In defining the HDL description, a complete block description, along with signal names, must be generated. Figure 19 illustrates an HDL block-level description of the PIPE LSIC.

The layout schematic verification shown in Figure 17 was used on the PIPE final layout. There were no catastrophic layout errors. Approximately 5,000 transistors were processed in the HDL software routine. A transistor size error in the clock driver was discovered during schematic verification but computer analysis showed no significant performance degradation. No other errors were found.

In anticipation of receiving processed parts, the slice-level test effort was restarted using the Texas Instruments advanced components tester (ACT). The first test involved continuity and power supply checks. Next, the controller was checked for data valid output involving clock driver and controller functionality. Finally, the EPROM was tested: all bits were checked for an erased state, random pattern

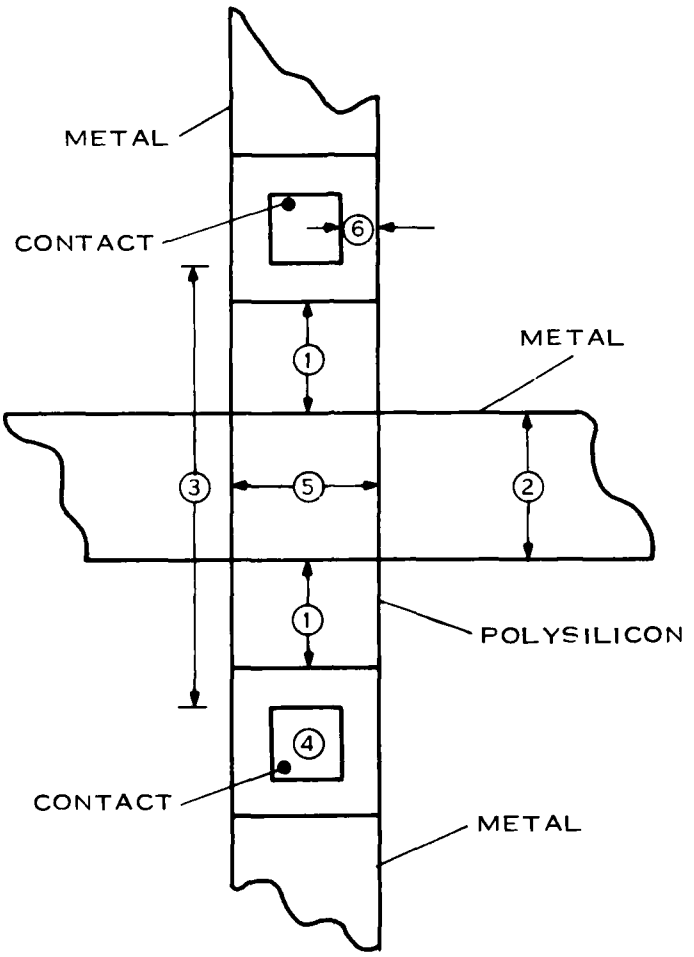


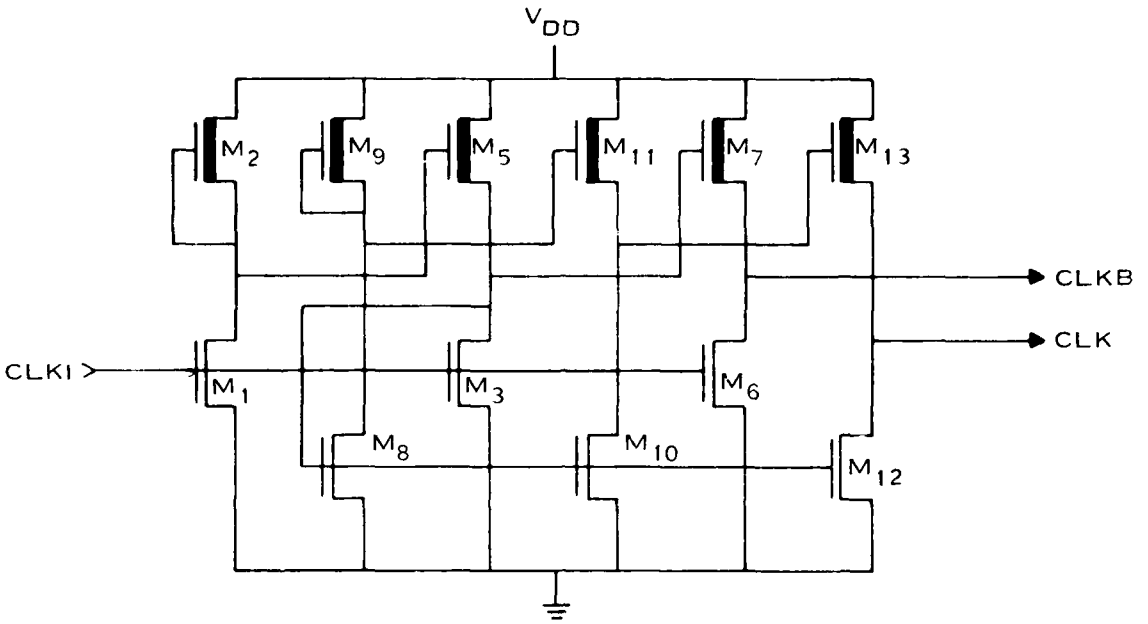
Figure 16. Layout Rule Check

verification made, and all bits programmed to a low. Devices passing the slice-level probe were scribed, broken, and bonded into 64-pin dual in-line packages. Detailed evaluation was performed using all I/O pads on the PIPE LSIC.

4. Second-Pass Results

Second-pass processing of the PIPE LSICs was completed on 28 January 1982.

Before application of the protective overcoat, two slices of LSICs were obtained for preliminary evaluation. Figure 20 shows the transistor characteristics of an enhancement and depletion mode transistor from the preliminary slice evaluation. The measured thresholds were +0.85 V and −2.7 V; the




```
BLOCK CLOCK;
(* PIPE2 CLKI CLOCK DRIVER *)
   CLKI @ INPUT;
   (CLKB, CLK) @ OUTPUT;
   STRUCTURE
      M01:NP  C4, CLKI, GND, BULK, 10, 0.2;
      M02:ND  VDD, C4, C4, BULK, 1.6, 0.4;
      M03:NP  C5, CLKI, GND, BULK, 16, 0.2;
      M05:ND  VDD, C4, C5, BULK, 8, 0.4;
      M06:NP  CLKB, CLKI, GND, BULK, 120, 0.2;
      M07:ND  VDD, C5, CLKB, BULK, 20, 0.3;
      M08:NP  C8, C5, GND, BULK, 2, 0.2;
      M09:ND  VDD, C8, C8, BULK, 0.8, 0.4;
      M10:NP  C9, C5, GND, BULK, 4, 0.2;
      M11:ND  VDD, C8, C9, BULK, 2, 0.4;
      M12:NP  CLK, C5, GND, BULK, 50, 0.2;
      M13:ND  VDD, C9, CLK, BULK, 20, 0.3;
END CLOCK;
BLOCK NP GENERIC;
```

Figure 17. Clock Block Schematic (Left) and Description (Right)

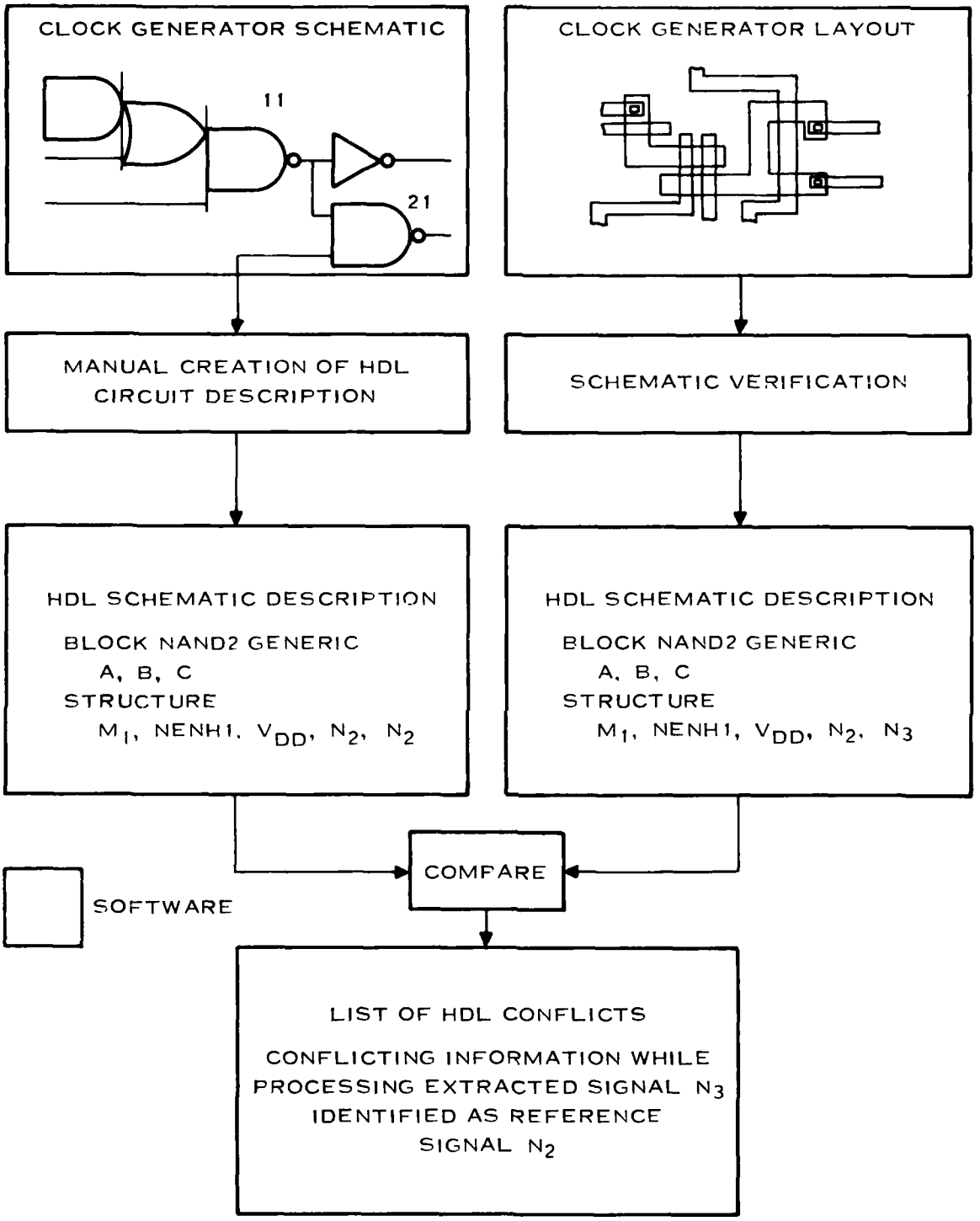


Figure 18. Verification Software Flow

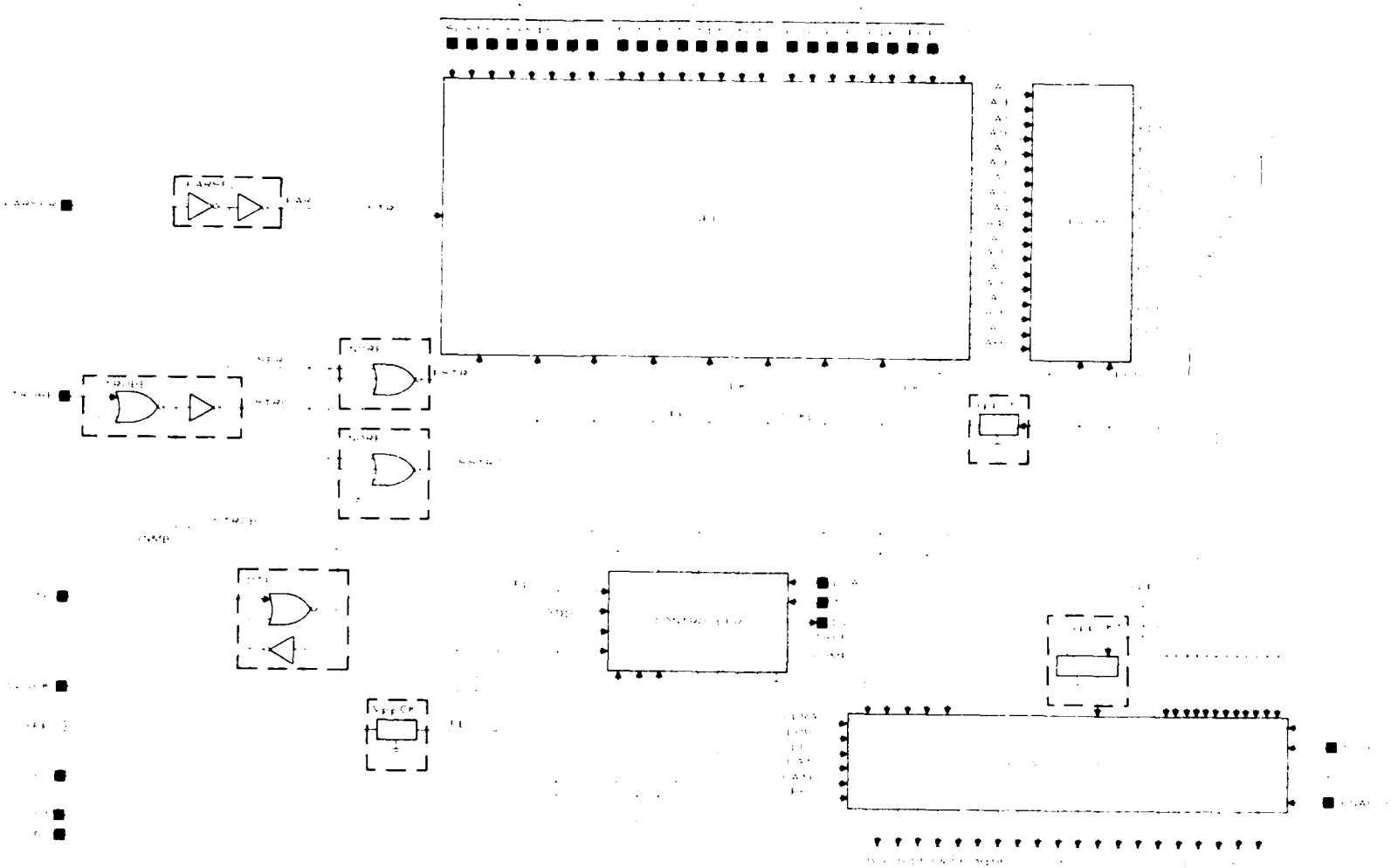
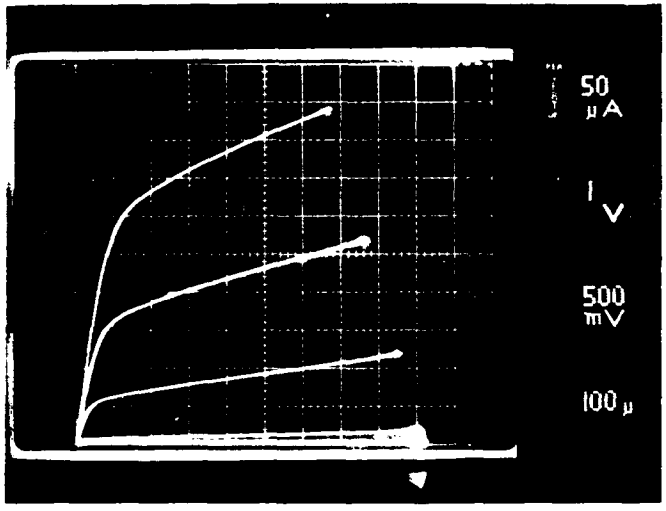


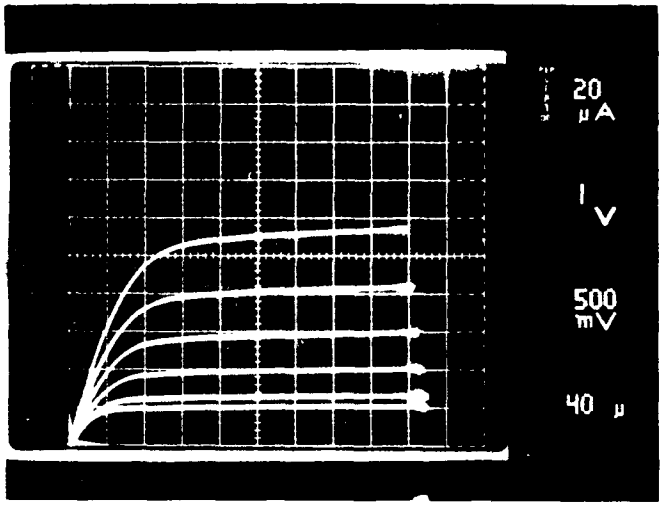
Figure 19. HDL Block-Level description of PIPE LSIC



ENHANCEMENT DEVICE

$V_T = 0.85$

W/L = 1.0/0.2



DEPLETION DEVICE

$V_T = -2.7V$

W/L = 1.0/0.4

Figure 20. PIPE LSIC Transistor Characteristics

design values were 0.80 V and −3.0 V, respectively. During the second pass, then, the thresholds were slightly closer to the design values than during the first pass. Figure 21 is a microphoto of the redesigned PIPE LSIC.

Each section was evaluated starting with circuits in which there had been design errors. First, the TTL-to-MOS clock driver was investigated. Figure 22 shows actual operation of the clock driver at 10 MHz. The waveforms appear somewhat degraded because of test setup and probe parasitics.

The next section evaluated was the shift register controller. Operation at 10 MHz is shown in Figure 23. The controller generates the parallel load, clear accumulate, latch accumulate, and data valid. The clock is the on-chip clock and the load is eternal to the chip. The power reset and the many NOR buffers used in the circuit were functional. A small problem was found with the data valid buffer. Series resistance in the output line prohibited a full TTL output level. However, using a pullup resistor or bonding closer to the driver improved the integrity of the pulse.

Next, operation of the tristate output latch was checked and found fully functional. Figure 24 shows an enabled tristate output with the input low and tristate pulse as input. Note that the tristate output buffer is of the inverting type.

The shift and accumulate was then checked. With the output of the PIPE memory erased to all digital 1's and the controller set for 8-bit operation, the controller was run and the shift and accumulate checked. The easily calculated result agreed with the output of the shift and accumulate and proved that the design errors had been successfully corrected.

Next, the input section, which had proved operational on first pass, was evaluated in detail. Figure 25 shows its operation at a 10-MHz clock rate. There are nine input latches with multiplexers to allow either parallel or serial input data and nine parallel-to-serial shift registers to convert the bit parallel words into bit serial format for addressing the memory. By operating the PIPE LSIC in the serial mode and strobing the input latches nine times, the 8-bit data at the serial port (1 0 1 0 1 1 0 0 for this case) is clocked through all the input latches and multiplexers. When the load pulse goes high, the bit parallel word is converted into a bit serial word beginning with the MSB.

The last circuit to be evaluated was the PIPE EPROM. The memory which was functional on the first pass, thus precluding redesign, was checked for access times, which is important to the overall operational speed of the PIPE LSCI. Worst case measurements were made and the results are indicated in Figure 26 that shows an address pulse with associated memory output. In addressing a high bit, the memory responded in 50 ns; when addressing a low bit, however, the time increased to 170 ns. This window is dependent on the memory cell (FAMOS) threshold. Ideally, the high and low access times should be identical, which would yield an overall access time of 110 ns.

Final testing of the PIPE LSIC was as a whole unit. All circuit blocks functioned together, and all timing proved correct. Erasure and reprogramming of the EPROM was confirmed. An operating frequency slightly above 10 MHz was demonstrated by all sections except the EPROM, which was slower than expected.

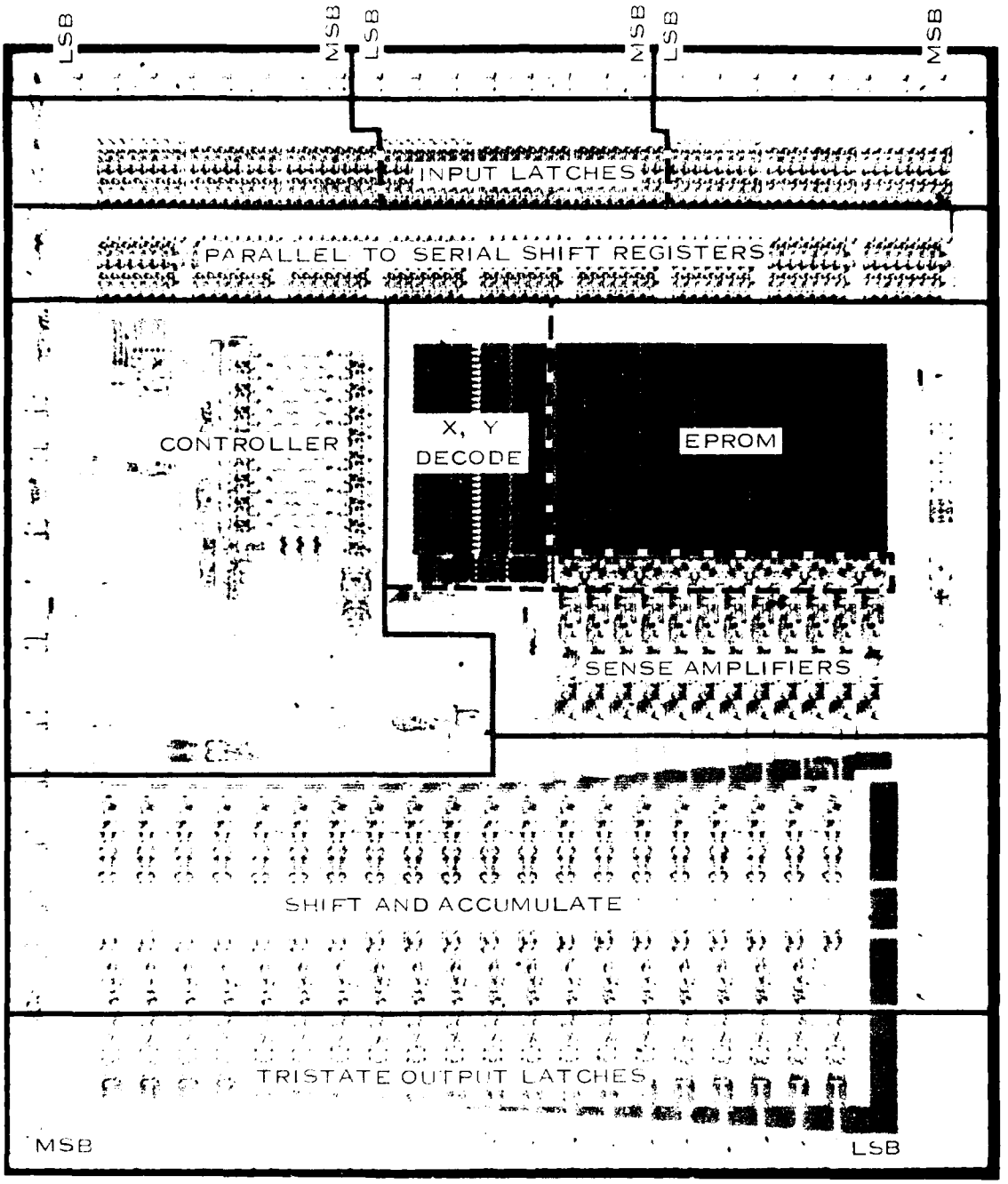
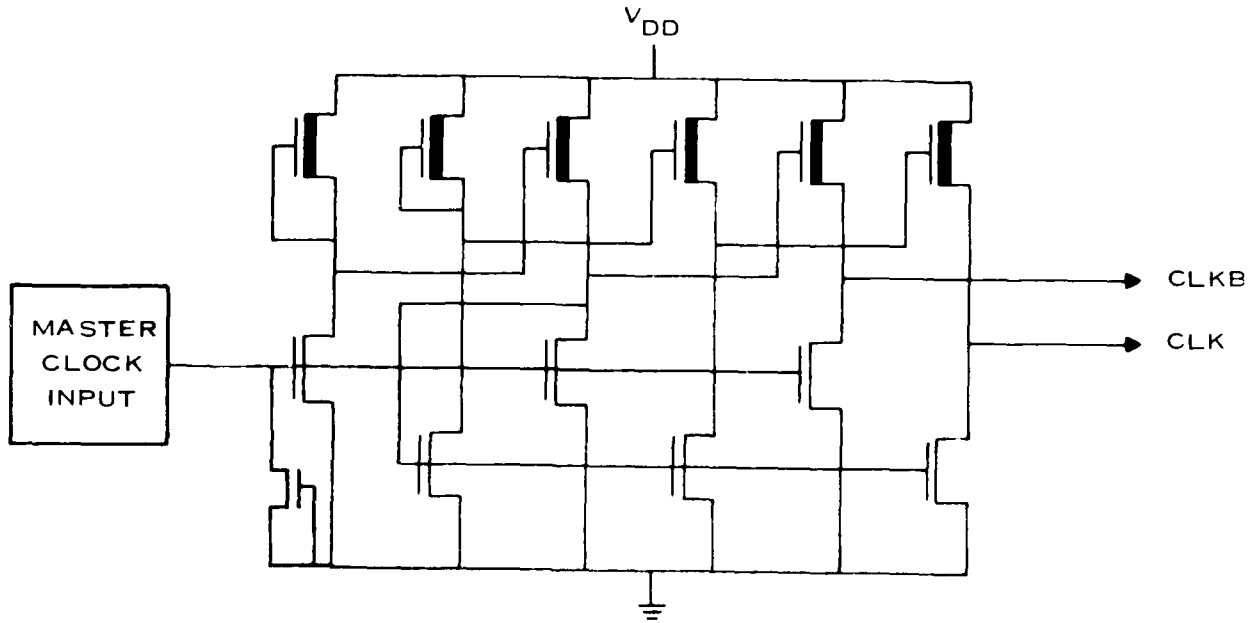


Figure 21. Microphoto of PIPE LSIC



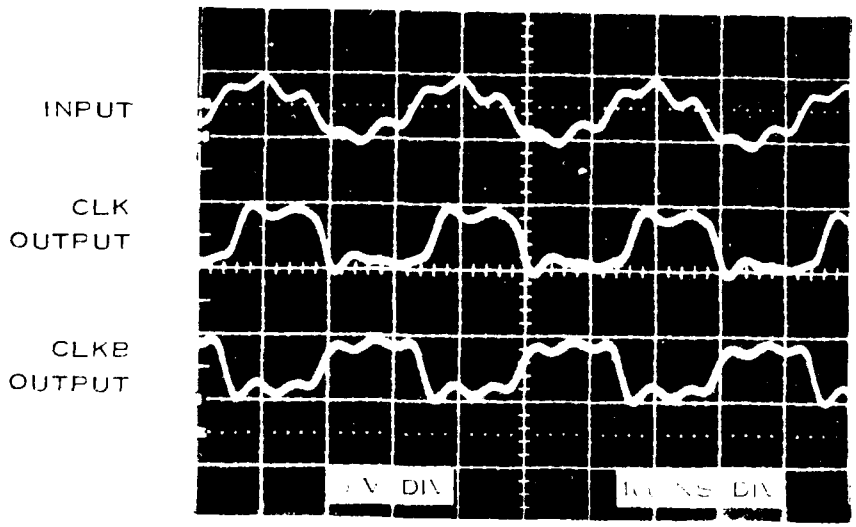


Figure 22. TTL-to-MOSS Clock Driver

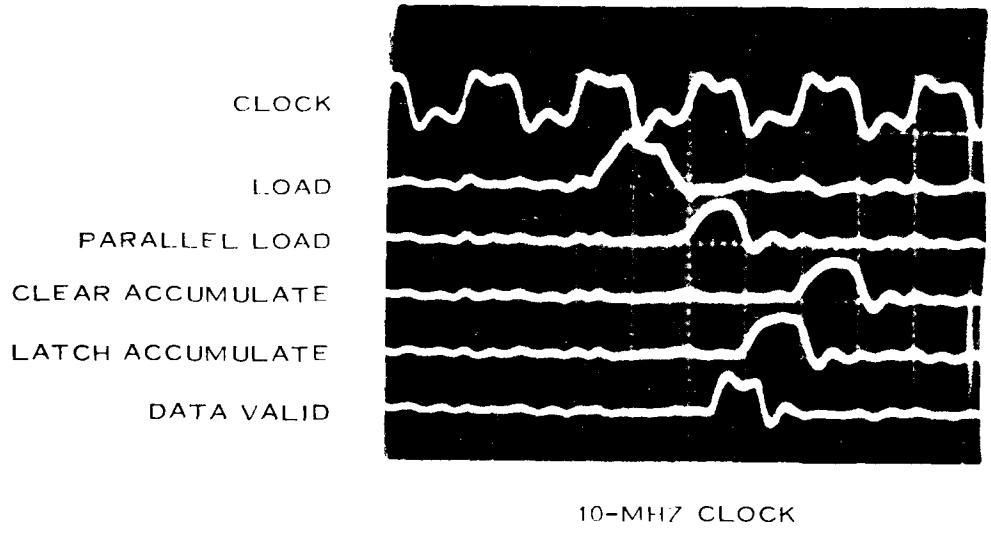


Figure 23. Operation of PIPE LSIC Shift Register Controller

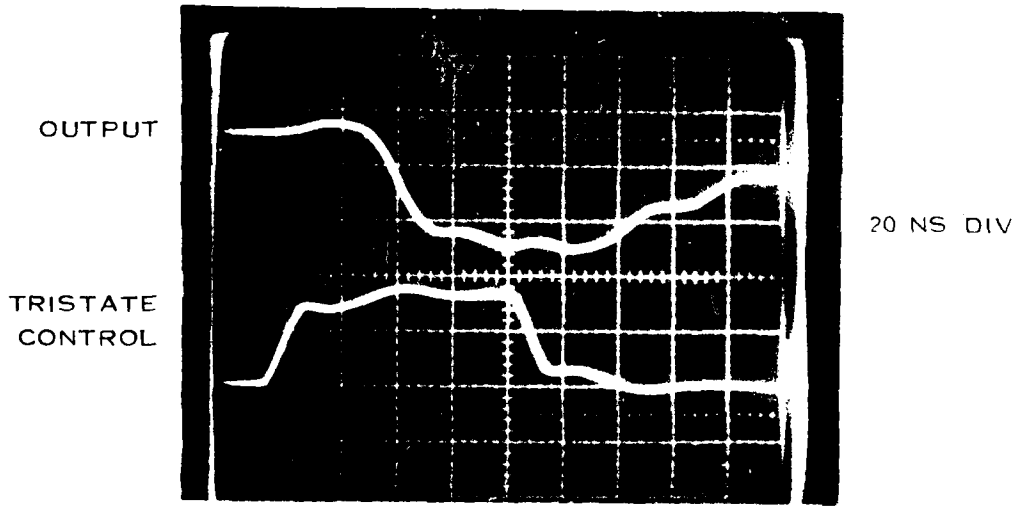
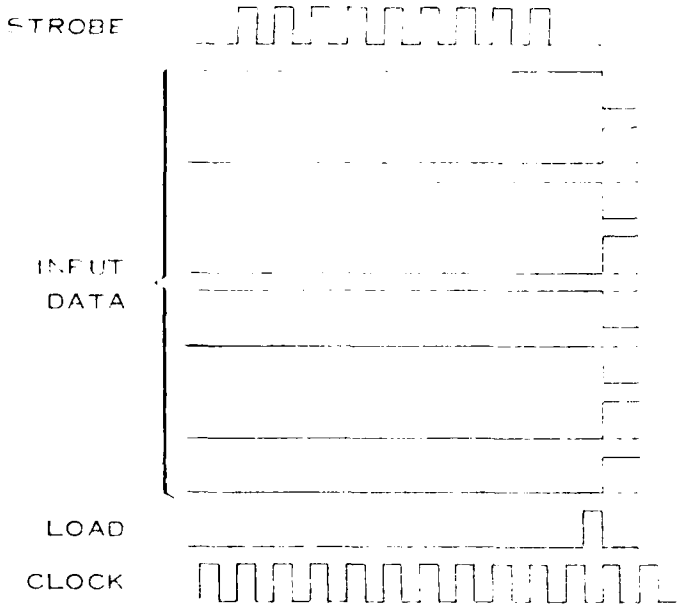


Figure 24. Tristate Operation



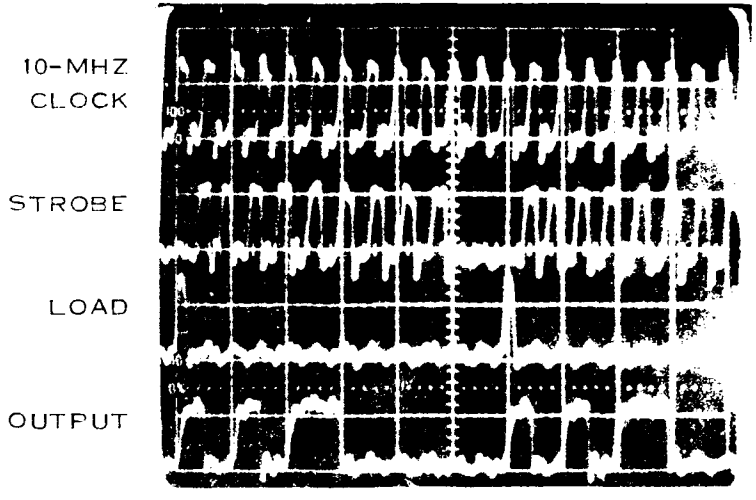


Figure 25. Input Latches: Parallel-to-Serial Shift-Register Operation

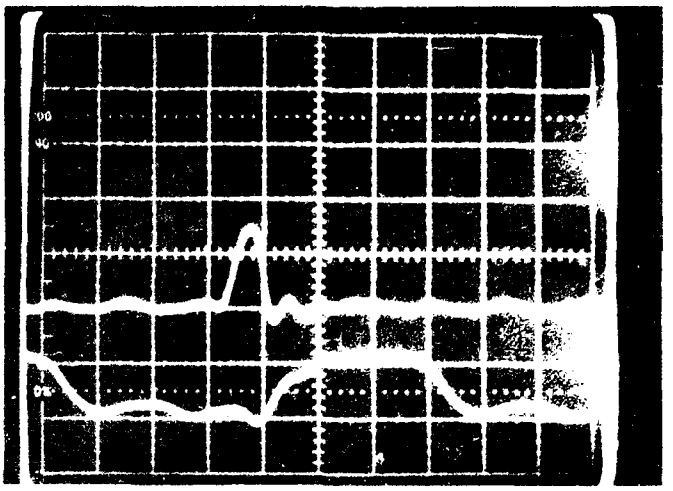


Figure 26. Memory Access Times

The LSIC's demonstrated power-supply sensitivity after initial operation. Operation was enhanced by running the V_{DD} supply at 5.5 V. This voltage sensitivity problem exists in the EPROM access times. Data appear at the output of the EPROM at slightly different times because of the bit path lengths. Operating at a higher voltage improves overall memory access time and eliminates missing bits by effectively changing the threshold-level detection point of the sense amplifier.

5. Processing and Packaging

Processing was begun on 12 December 1981 on 15 slices, 12 of which were successfully finished on 28 January 1982. Probe yield was good, averaging around 50 percent. Overall packaged device yield showed a 10-percent loss, resulting in a 40 percent overall slice-to-package yield. This high yield was the result of the NMOS 5-μm process, which by today's standards is old; 3-μm processes are in production today, and 2-μm and 1-μm processes are in preproduction development.

A 64-pin hermetic package with a UV lid for memory erasure was used for the PIPE LSIC's. Figure 27 is a picture of the final packaged part. The PIPE LSIC measures 240 × 270 mil and contains more than 11,000 MOS transistors.

6. Summary

The objective of the PIPE program was the design and development of a general-purpose, programmable, digital integrated circuit capable of multiple signal-processing functions.

Over the last 20 years, the semiconductor industry has progressed steadily in its effort to achieve greater capability from semiconductor and other device technologies at lower costs. Products of this effort include increased functional densities (more capability in smaller volume), improved performance power ratios, higher processing throughput rates, improved reliability, and many more. In 1978 when the PIPE

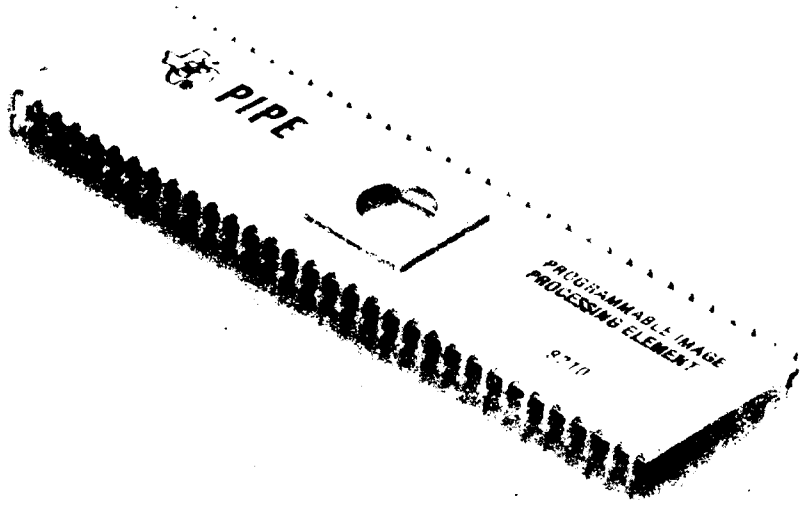


Figure 27. PIPE LSIC in 64-Pin Dual In-Line Package

LSIC development began, 5-μm technology was the state of the art in production technology. Since then, 3-μm technology has moved to the production lines and 1-μm technology is being developed. Using the technology that is available today, the overall operating speed of the PIPE LSIC could be significantly enhanced.

The PIPE LSIC development demonstrates the feasibility of using more than 11,000 MOS transistors in implementing a ROM accumulate (RAC) processor on a single LSIC. It provides a user-oriented vehicle for testing various image-processing algorithms. The present 5-μm EPROM version of the PIPE LSIC operates at a maximum clock rate of 5 MHz, which is owing totally to EPROM access times. Using 2- to 3-μm technology and replacing the EPROM with ROM could result in a PIPE LSIC capable of 20-MHz clock rates. Table 5 summarizes chip performance and power requirements. Table 6 is a pinout assignment list for the PIPE LSIC (data inputs A, B, and C are designated by P, L, and S, respectively, to avoid confusion with the EPROM programming address), and Table 7 lists the controls.

B. PIPE EPROM PROGRAMMER

To program and/or verify the PIPE LSIC EPROM, a programmer capable of interfacing to a Digital Equipment Corporation PDP-11 computer via a DR11-C interface or a Texas Instruments 990/10 computer through a 16-bit CRU I/O interface was designed and fabricated. In the simplified block diagram of the EPROM programmer, Figure 28, lines OD0–OD15 are 16 data lines that transfer data from the host computer to the programmer, lines ID0–ID15 are 16 data lines that transfer data from the programmer to the host computer, and the lines NEW DATA, CS1, and CS2 are control signals that determine the operation of the programmer. If a DR11-C interface is used, control signals CS1 and CS2 correspond to

TABLE 5. PIPE CHARACTERISTICS

	Maximum	Minimum
Maximum operating voltage	10 V	4.5 V
Maximum programming voltage	35 V	17 V
Maximum strobe frequency	12 MHz	–
Maximum clock frequency*	12 MHz	1 kHz
Typical EPROM access time	170 ns	–
Power requirements	800 mW at 5 V	–
Memory erase time (2537 Å at 15 W-s cm^{-1})	–	40 minutes

*Dependent on EPROM access time and mode of operation.

bit 0 (CSR0) and bit 1 (CSR1), respectively, of the control and status register. These bits can be loaded or read from the UNIBUS. The control signal NEW DATA is a 400-ns-wide positive pulse generated by the DR11–C interface when information is loaded into the OUTPUT BUFFER REGISTER from the UNIBUS. If a 16-bit CRU I/O interface is used, the user must generate the control signals NEW DATA, CS1, and CS2.

The programmer has two modes of operation—program and verify—that are determined by the state of the control signal CS2. Since the PIPE EPROM is organized as 512 × 12, programming requires 12 bits of data and 9 bits of address. The controller uses some of the 16-input data lines (OD0–OD15), some of the 16-output data lines (ID0–ID15), and some of the PIPE LSIC outputs during programming and verification.

To program a word into the PIPE LSIC EPROM, address, data, and programming voltage are required. The program mode is defined by a logical high state on control signal CS2; special power-on circuitry is included in the control logic to force the output of the CS2 buffer to a low state, thus preventing accidental programming of an EPROM location when power is initially applied.

To load the 9-bit EPROM address into the address latches, the address word is output from the host computer on lines OD0–OD8. The MSB of the 16-bit output lines, OD15, is also set high and used by the control logic in conjunction with the NEW DATA control signal to clock the address into the address latch. The address is latched into the address latches on the high-to-low transition of the NEW DATA control signal. The CS2 is used to enable the address latch. During the program mode, the address latch is constantly enabled.

After the address has been latched, the 12-bit EPROM data is latched into the data latch. This is accomplished by setting data line OD15 to a logic low level, outputting the 12-bit data on data lines OD0–OD11, and pulsing the NEW DATA control line. Again, the data is latched into the data latches on the high-to-low transition of the NEW DATA control line. Control signal CS2 is also used to enable the data latch; therefore, during the program mode, the data latch is constantly enabled.

TABLE 6. PIPE PACKAGE PINOUT

Function	Pin				Pin	Function
GND	1	P	A	I	64	T1
T0	2	I	F	I	63	T2
S7 (A6)	3	I	W	I	62	T3
S6 (A7)	4	I	A	I	61	T4
S5 (A8)	5	I	L	I	60	T5 (A5)
S4	6	I		I	59	T6 (A4)
S3	7	I	P	I	58	T7 (A3)
S2	8	I	I	I	57	P0
S1	9	I	P	I	56	P1
S0	10	I	E	I	55	P2
Parser	11	K	2	I	54	P7 (A0)
V_{DD}	12	P		I	53	P6 (A1)
Strobe	13	C	L	I	52	P5 (A2)
CLKI	14	C	S	I	51	P4
DTF	15	K	I	I	50	P3
TCDB	16	K	C	?	49	Not used (DMA)
V_{PP}	17	P		P	48	V_{PP}
LOAD	18	C	6	K	47	TCCB
B0	19	K	4	P	46	GND
B1	20	K		P	45	V_{DD}
B2	21	K	L	IO	44	D3
DV	22	O	E	IO	43	D2
ENA	23	K	A	IO	42	D1
V_{DD}	24	P	D	IO	41	D0 LSB
D19 MSB	25	O		IO	40	D4
D18	26	O	H	IO	39	D5
D17	27	O	E	IO	38	D6
D16	28	O	A	IO	37	D7
D15	29	O	D	IO	36	D8
D14	30	O	F	IO	35	D9
D13	31	O	R	IO	34	D10
D12	32	O		IO	33	D11

(I = input, O = output, IO = input output, C = clock, K = control, P = power)

TABLE 7. CONTROL DEFINITION

Control Line(s)	Function
Word length (3-bit BCD code)	Defines word length in bits of input data*
Parallel/serial	Determines mode of chip operation: 3 × 3 or 9 × 1
Master clock	A square-wave clock provided for system timing
Load	Initiates parallel-to-serial data conversion
Input strobe	Indicates valid input data and latches it in input latches
2's complement data	Defines signed or unsigned magnitude data operation
Enable	Tristates or enables output bus
V_{DD}	Single + 5-V operating supply
V_{PP}	Normally at 5 V but taken to 25 V for EPROM programming
Data valid	Output signal indicating complete computation
2's complement coefficients	Sets sign bits of output word
DTF	Inhibits input strobe during parallel load operation

*Word length of 1 used for memory verification.

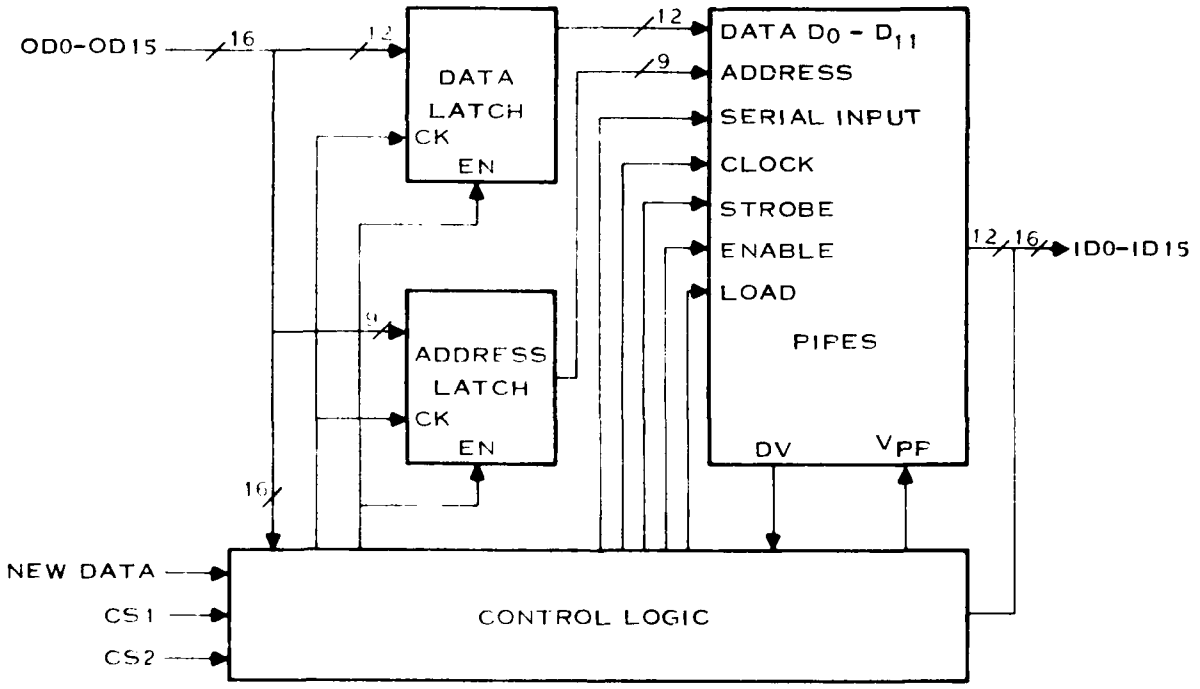


Figure 28. Block Diagram of PIPE EPROM Programmer

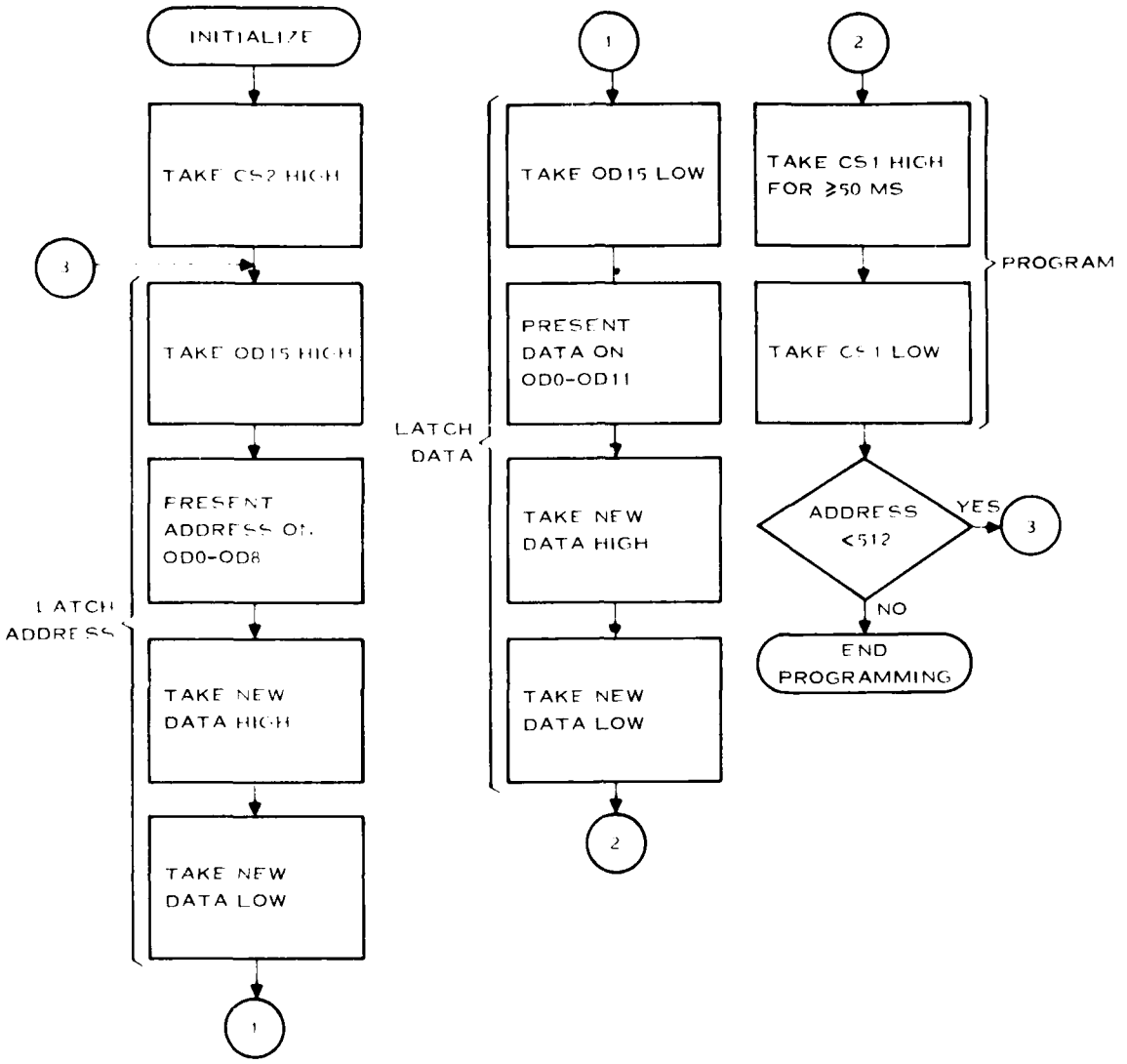


Figure 29. PIPE EPROM Programmer Program Mode

To program an EPROM location defined by the 9-bit address with the data in the data latches, the programming voltage V_{pp} is taken from its normal 5-V level to the programming level of 25 V for a minimum of 50 ms. When control signal CS1 is taken high, V_{pp} is taken to 25 V, causing a multiplexer internal to the PIPE LSIC to select the 12 LSBs of the PIPE's 20-bit output as EPROM data inputs and the 3 MSBs of each of the three PIPE inputs as EPROM addresses. After 50 ms, CS1 is taken low and the data word has been programmed. The next address and data can now be latched and programmed. Figure 29 summarizes the EPROM programmer's mode of operation. After all 512 EPROM words are programmed, CS2 is taken low, thus disabling the address and data latches. The PIPE LSIC inputs and outputs can then be used to read the contents of the EPROM to verify correct programming.

Reading the contents of the PIPE EPROM is much more difficult than programming because verification requires dynamic operation of the PIPE LSIC. When operating the PIPE LSIC in the serial mode with 1-bit input data, an EPROM address can be strobed into the input latches of the PIPE LSIC; after three clock cycles, the 12 LSBs of the PIPE output represent the data at the EPROM address defined by the input data.

When control signal CS2 is low, the PIPE programmer is in the verify mode of operation. A parallel-in/serial-out shift register within the control logic hardware is loaded with the 9-bit address on lines OD0–OD8 when data line OD9 is high and control line NEW DATA is pulsed. Data line OD9 is then set to a low level, putting the shift register in a shift mode. The first of nine 1-bit words is then available at the PIPE LSIC serial input and strobed into the PIPE input latch by pulsing control signal CS1, i.e., taking CS1 high and then low. (CS1 controls the PIPE LSIC strobe line.) The next 1-bit word is shifted out of the shift register and strobed into the PIPE LSIC by pulsing NEW DATA, then pulsing CS1. This procedure is repeated until all nine 1-bit words of the desired address have been strobed into the PIPE input latches. The PIPE LSIC is issued a load pulse and clocked by the control logic. Assuming that the programmer's clock is faster than the host computer, the latter can issue a read instruction, and the output of the PIPE LSIC can be read. An enable generator internal to the control logic enables the PIPE's tristate outputs. Data line OD10 is taken high, and the PIPE denoted by data lines OD11–OD13 (i.e., binary equivalent for the PIPE No. 0–7) is enabled for the host computer to verify. If the operator only wants to verify one PIPE LSIC, input data line ID13 can be set low through a front-panel switch and only PIPE No. 0 will be enabled. If eight PIPE LSICs are to be verified, the panel switch is set high (ID13 is high), and the enable generator will sequentially enable the PIPE LSICs, beginning with device 0.

After the PIPE device(s) has been verified, the next address is loaded in the control logic shift register and the process repeated. Figure 30 summarizes the verification mode. After all 512 EPROM locations have been verified, all data and control signals are taken low.

C. DEMONSTRATION BRASSBOARD

1. Overview

To demonstrate the PIPE LSIC versatility, a flexible brassboard operating in or near real-time was developed. The design goals of the brassboard were as follows:

- Feature standard RS-170 composite video input and output
- Provide 10-MHz data rate (512 × 512 display)
- Provide serial or three parallel (vertically sequential) words
- Provide and control signals (clock, strobe, load, etc.,) to PIPE LSIC
- Provide magnitude, maximum, threshold, and no-op postprocessing functions

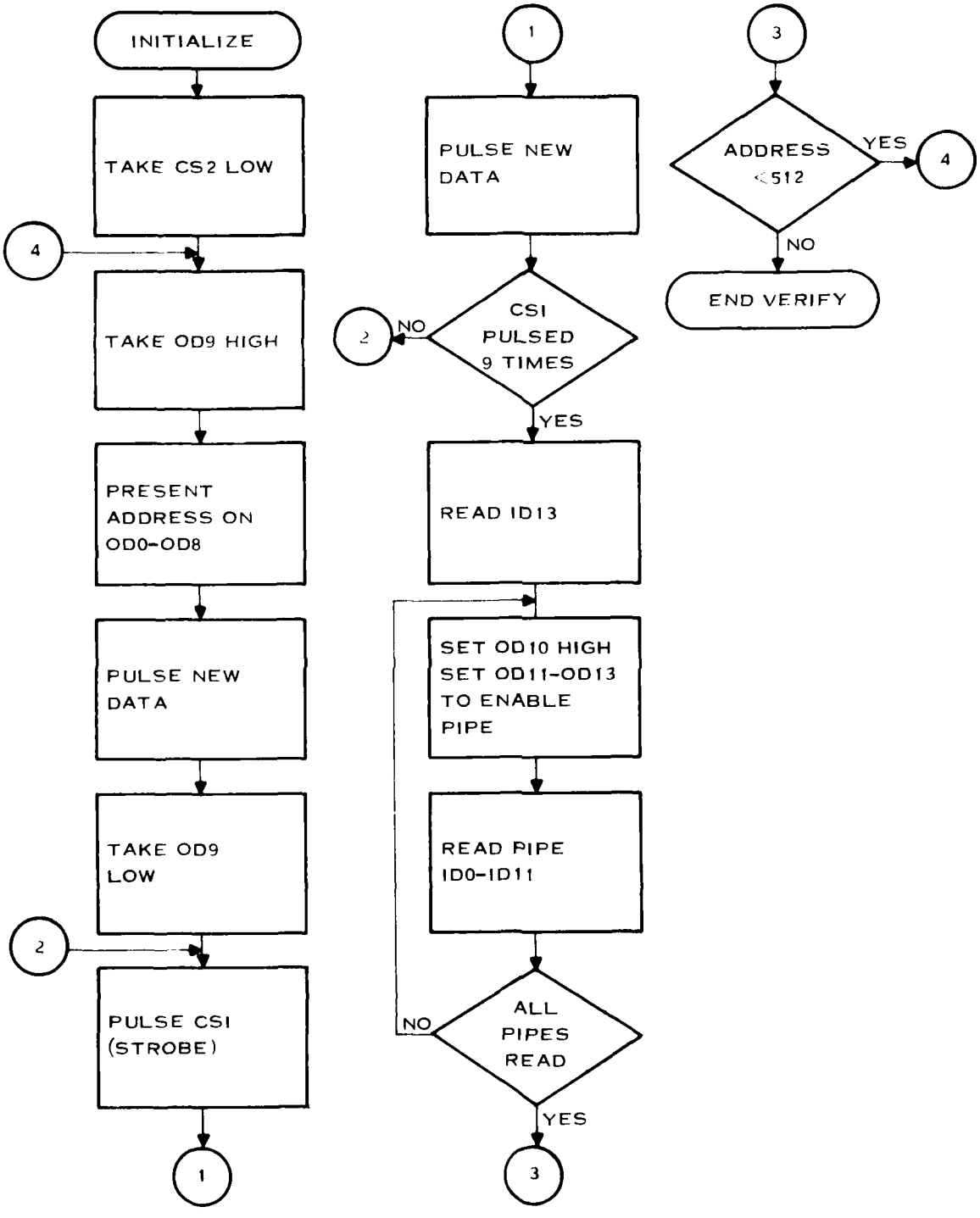


Figure 30. PIPE EPROM Programmer Verify Mode

- Demonstrate various operations
  - Differential edge detector (Prewitt, Sobel, etc.)
  - Template-matching edge detector (Compass, Kirsch, etc.)
  - Low-pass filter.
- Provide flexibility to allow future hardware demonstration.

The most important goal was the flexibility to demonstrate future hardware developments.

The demonstration brassboard, Figure 31, is completely self-contained, accepts single-line video as input, and displays processed results on a standard TV monitor for evaluation. The brassboard will operate the PIPE LSIC in both its serial and parallel modes and demonstrate its processing of vector transforms and neighborhood operators. The analog video input is quantized to 8-bit precision and stored in the frame buffer memory, which forms the frame images from the time interlaced video fields. Images composed of 512 by 512 8-bit pixels can be processed at frame rates determined by the PIPE LSIC throughput, buffer memory speed, brassboard architecture, and the algorithm being computed. Pixel processing rates for the PIPE LSIC are limited by the EPROM access time.

Eight PIPE LSIC's are used in the brassboard. For the 3×3 differential edge detectors, four PIPE LSIC's calculate the horizontal response while the other four are calculating the vertical response. The template-matching edge detectors also require eight PIPE LSIC's for maximum throughput, with one template assigned to each PIPE. The output of the PIPE LSIC's is processed according to the operation selected (e.g., calculating the magnitude and orientation for the differential edge detectors or finding the maximum response for template-matching edge detectors). A minimum amount of interface between the user and the PIPE LSIC is required to communicate the type of operation to be performed, the format of input data, etc. This interface is implemented through a control panel for the demonstration brassboard. This control panel uses a 16-key calculator-style keyboard for command entry, a 24-character alphanumeric LCD display for displaying current operating parameters and prompting the user for new parameters, and a 3-digit thumbwheel switch for entering threshold levels. The user commands the brassboard to perform various operations by responding to seven prompts with seven single keystroke replies. These prompts query the user for operating parameters such as parallel or serial input, 2's complement data, 2's complement weighting coefficients, word length, weighting arrangement (i.e., do all eight LSIC's contain the same weights?), postprocessing operation (magnitude, maximum, or no operation), and sliding or nonsliding operation.

A display-refresh memory and digital-to-analog converter provide analog data in a standard TV-monitor format. Both the ADC and DAC are high-speed (10-MHz), 8-bit, commercially available components.

The brassboard is constructed from off-the-shelf components and standard wire-wrap techniques. The brassboard is functionally partitioned into 13 wire-wrapped boards, each measuring 7.3×7.0 in. and capable of containing up to 60 integrated circuits in 16-pin dual in-line packages. There is a 1:1 correspondence between the boards and the block diagram shown in Figure 31.

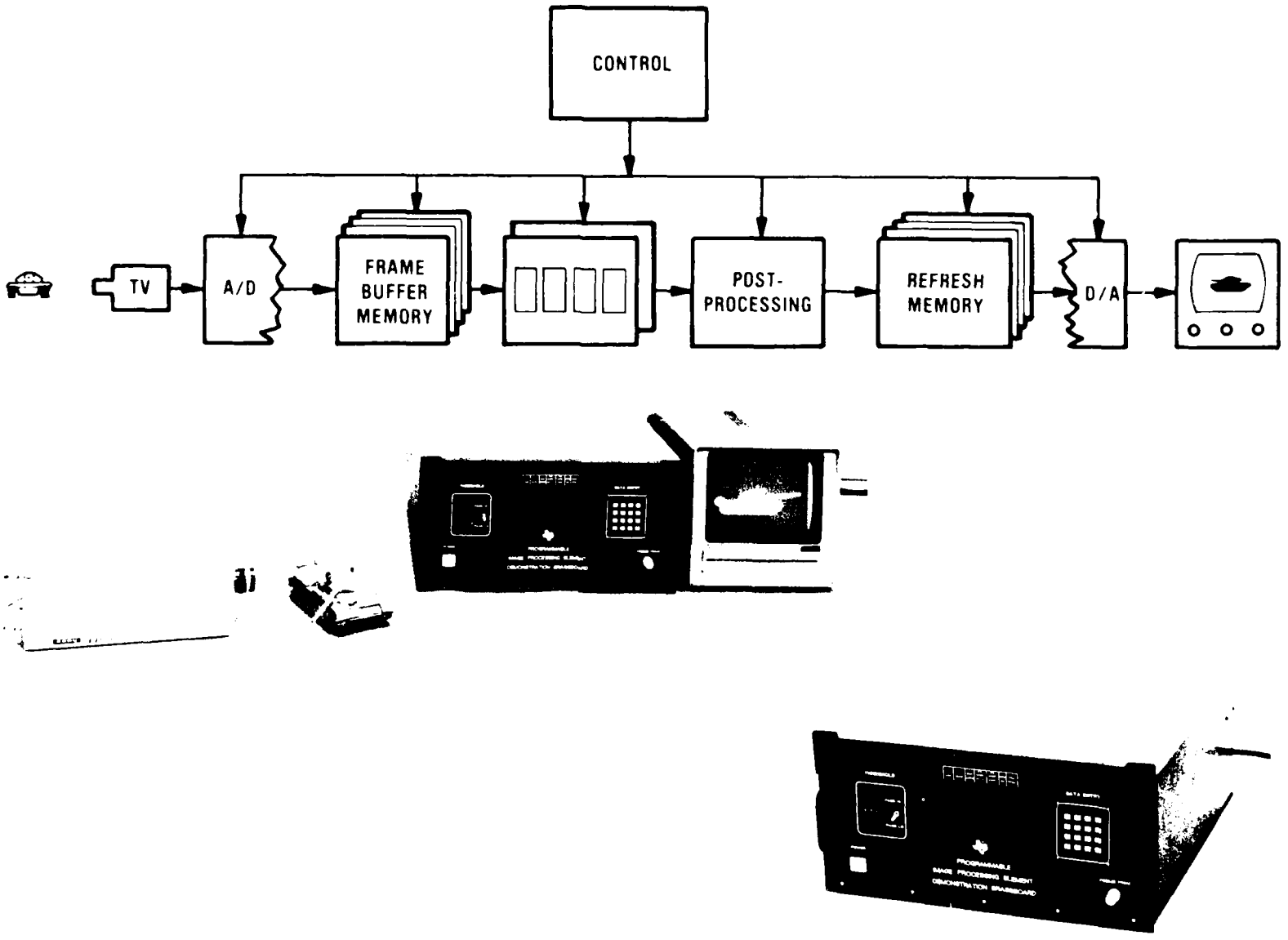


Figure 31. PIPE Demonstration Brassboard

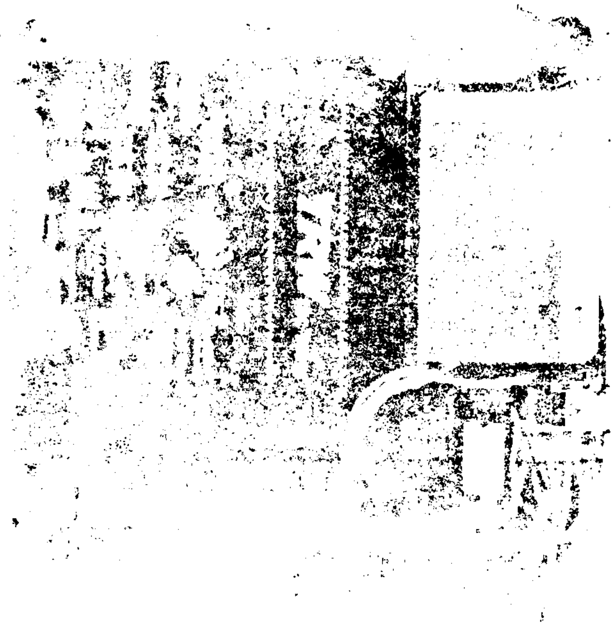


Figure [illegible] PIPE Demonstration Brassboard Analog Module

The following subsections [illegible] and design of the demonstration brassboard. Detailed logic schematics [illegible] in Appendix [illegible]

2. Analog-to-Digital and Digital to Analog Converters

The analog module [illegible] of the PIPE brassboard contains the ADC and the DAC. Combining both of these functions on the same [illegible] maximizes the isolation of composite video from other signals and provides [illegible] system performance.

The brassboard is designed [illegible] camera with a genlock option that permits the internal [illegible] pulse to be locked in phase with an external EIA standard RS-170 synchronization [illegible] the camera to the ADC. The ADC converts the standard RS-170 video [illegible] digital processing.

A commercially available [illegible] PCB, was selected because of its high speed and availability. This module [illegible] ADC [illegible] and gain adjustments, buffer amplifier and voltage [illegible]

A [illegible] controlled [illegible] is used on the output of the [illegible] digital data with other brassboard functions.

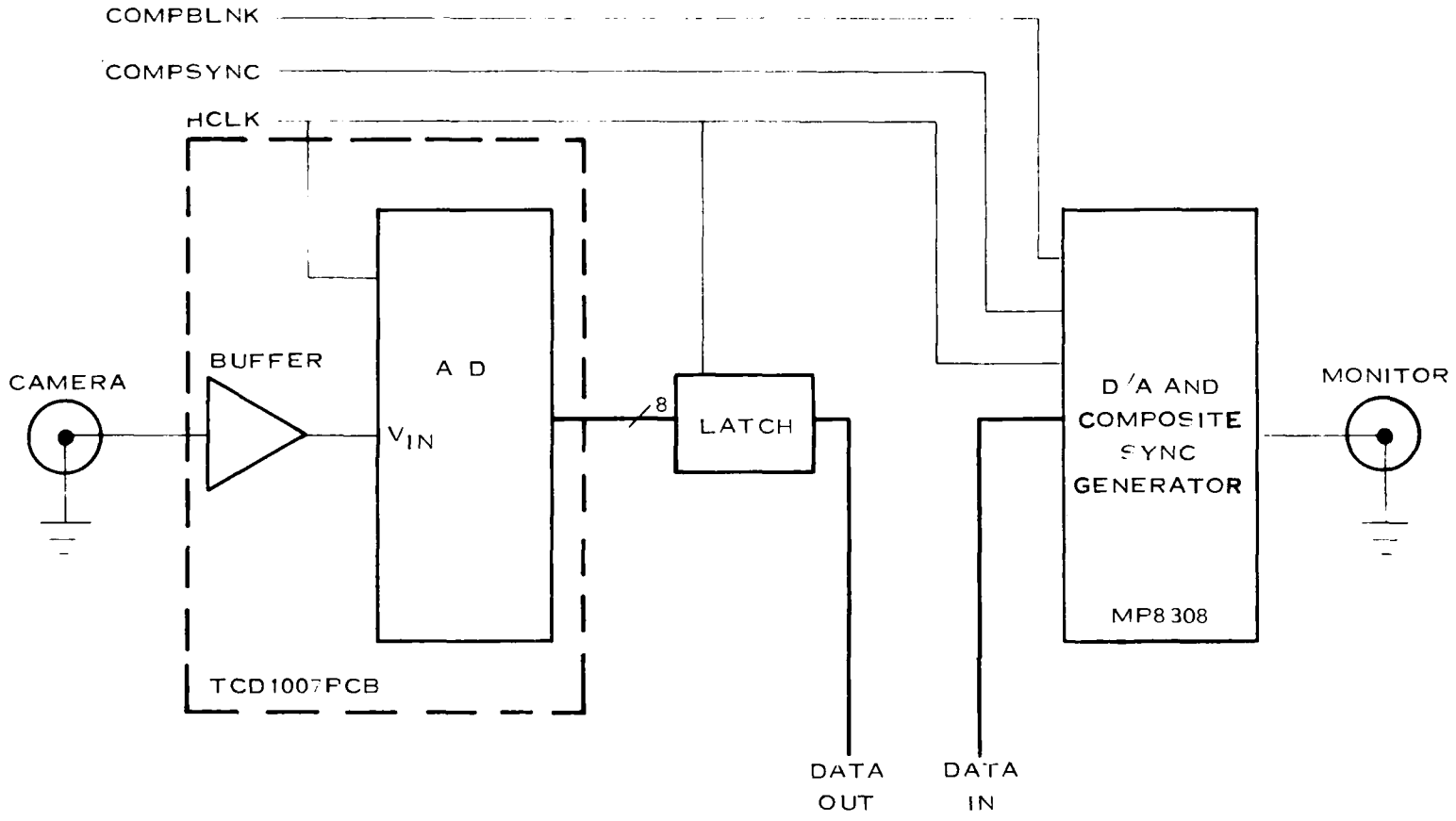


Figure 33. Analog Module of PIPE Demonstration Brassboard

The DAC on the brassboard's analog board is actually a combination of DAC and composite sync generator. This unit, an Analogic MP8308, accepts 8-bit digital data from the fresh memories' composite blanking ($\overline{\text{COMP BLNK}}$) and composite sync ($\overline{\text{COMP SYNC}}$) from the timing board and produces standard RS–170 composite video with 256 gray shades that will directly drive the composite video input of a television monitor.

The use of a commercially available ADC and DAC sync generator greatly simplified the design of these functions.

3. Buffer Memory

The buffer memory stores a complete video frame of two interlaced fields, each containing 256 lines with 512 pixels/line. The buffer memory is designed to capture data from the ADC at a 100-ns pixel rate and to provide vertically related pixels from three adjacent lines simultaneously as inputs to the PIPE LSICs. Data from memory is available also in serial format for demonstrating the PIPE LSIC's serial mode of operation.

As shown in the simple block diagram, Figure 34, the memory is partitioned into odd-field odd line, odd-field even line, even-field odd line, and even-field even lines. The memory design is based on the Intel 2118, 16k × 1-bit dynamic RAM (DRAMs), which requires a single +5-V power supply and dissipates 150 mW operating and 11 mW standby. The typical read/write cycle time of those DRAMs is 270 ns, but a special demultiplexing/multiplexing scheme permits using memories with access times of less than 100 ns. The buffer memory requires 128 (each 16k × 1) DRAMs to store an image of 512 × 512 × 8 bits. The addition of data registers, address generators, and multiplexers to provide additional versatility increased the number of components for the buffer memory to 240. The wire-wrap boards selected for fabrication of the brassboard accommodate 60 components; therefore, four boards (Figure 35), each representing 512 × 512 × 2 bits of memory, are required.

Figure 36 shows more detail of one buffer memory board (512 × 512 × 2 bits). Data received by the memory boards is input to a 4-bit serial-in/parallel-out (SIPO) shift register to reduce the required 10-MHz data rate to a 2.5-MHz or 400-ns memory cycle time. When the shift register is full, all four words are written to memory simultaneously. Control lines YO and ODDFLD determine the bank [i.e., odd-field odd line (OFOL), even-field odd line (EFOL), odd-field even line (OFEL), or even-field even line (EFEL)] in which the data is written. The seven address lines and control lines C1, C2, C3, and C4 determine the address within a given bank.

Control signal OUTLD loads 4 bits of memory data into a parallel-in/serial-out (PISO) shift register to multiplex the memory outputs. This is the inverse of the demultiplexing of the input data and restores the data rate to 10 MHz.

Because three adjacent lines of video are required simultaneously, three multiplexers and a register are used to select the correct line of data for a given output line ALN, BLN, CLN. The multiplexers are controlled by a 9-bit output select word generated on the timing and synchronization board. During

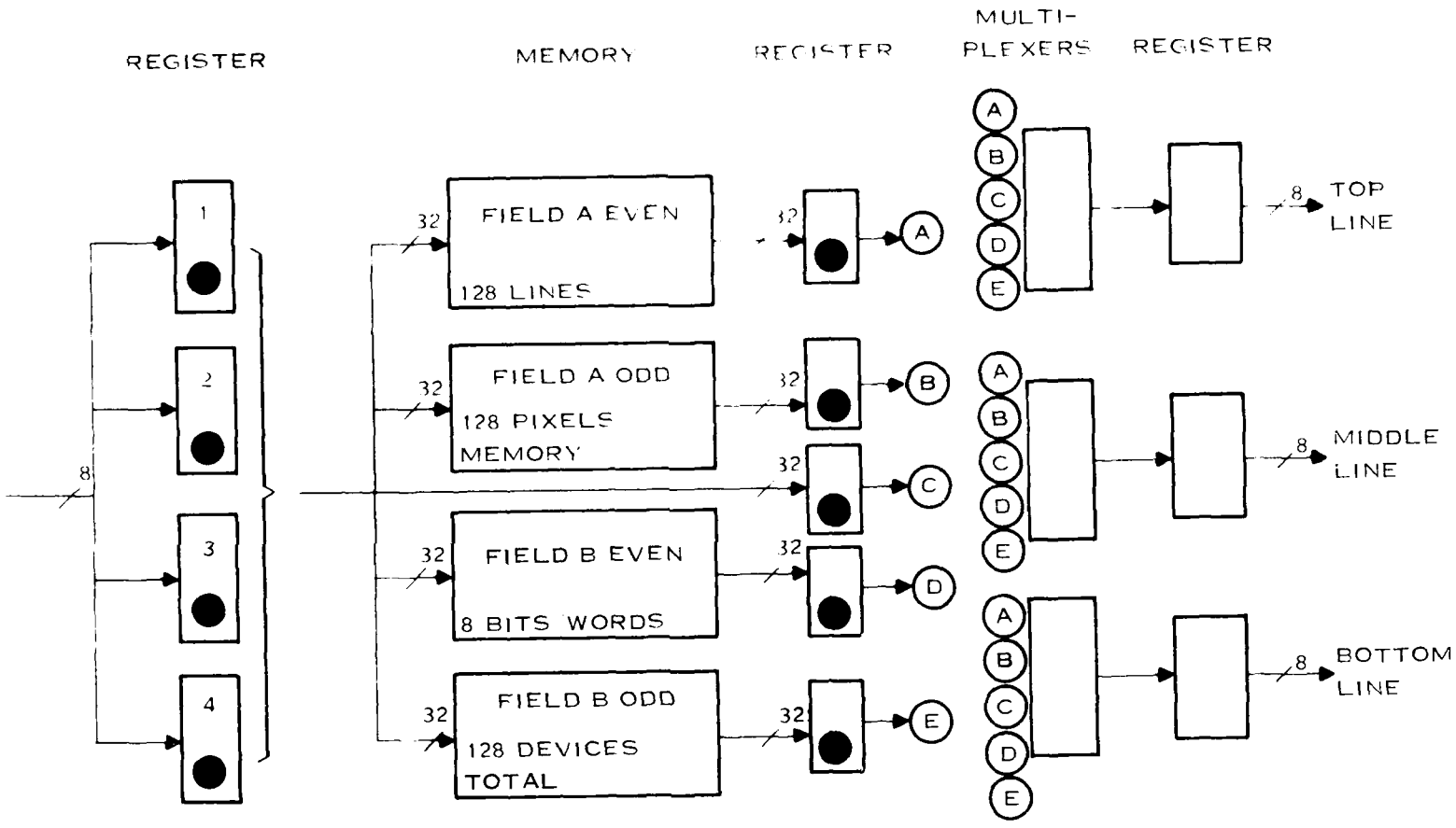


Figure 34. Buffer Memory of PIPE Demonstration Brassboard

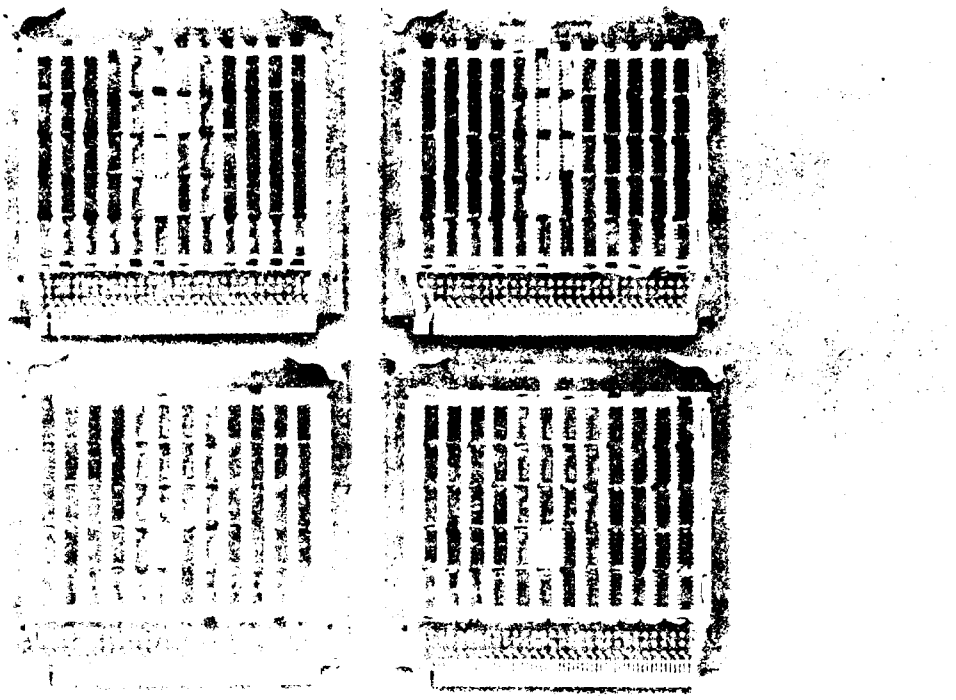


Figure 35. PIPE Brassboard Buffer Memory Boards

parallel operations, the BLN output is unstored "live" video; during serial operations, the CLN output represents unstored video. The memory boards also require row address strobe (RAS), column address strobe (CAS), and write (WR) control lines to address and write data properly into the DRAMs.

Figure 37 shows eight lines of standard raster scan video. Because of the time interlacing, Field A data must be written to memory before Field B data. The memory is partitioned to allow storage of four TV lines at the same y address, i.e., TV lines 0, 1, 2, and 3 at y address 0. Control lines YO and ODDFLD determine the specific DRAM to which data is written. For example, TV line 0 is stored at y address 0 in the odd-field odd line memories, which are the top row of memories in Figure 36; also, TV line 4 is stored in these memories at y address 1.

Reading data from the buffer memory is more complex. During a read operation, the y address must be modified to obtain three adjacent lines of TV video. Referring again to Figure 37, if data from TV line 2 is at output BLN (unstored video for parallel operations), data from TV lines 1 and 3 are at outputs ALN and CLN, respectively. In this case, no y address modification is necessary because all the data is at y address 0. If data from TV line 3 is at output BLN, the y address is 0 and no modification is necessary to obtain data from TV line 2 at output ALN. To obtain data from TV line 4 at output CLN, the y address of the OEOL memory bank must be incremented by 1. When TV line 4 is at output BLN, a more

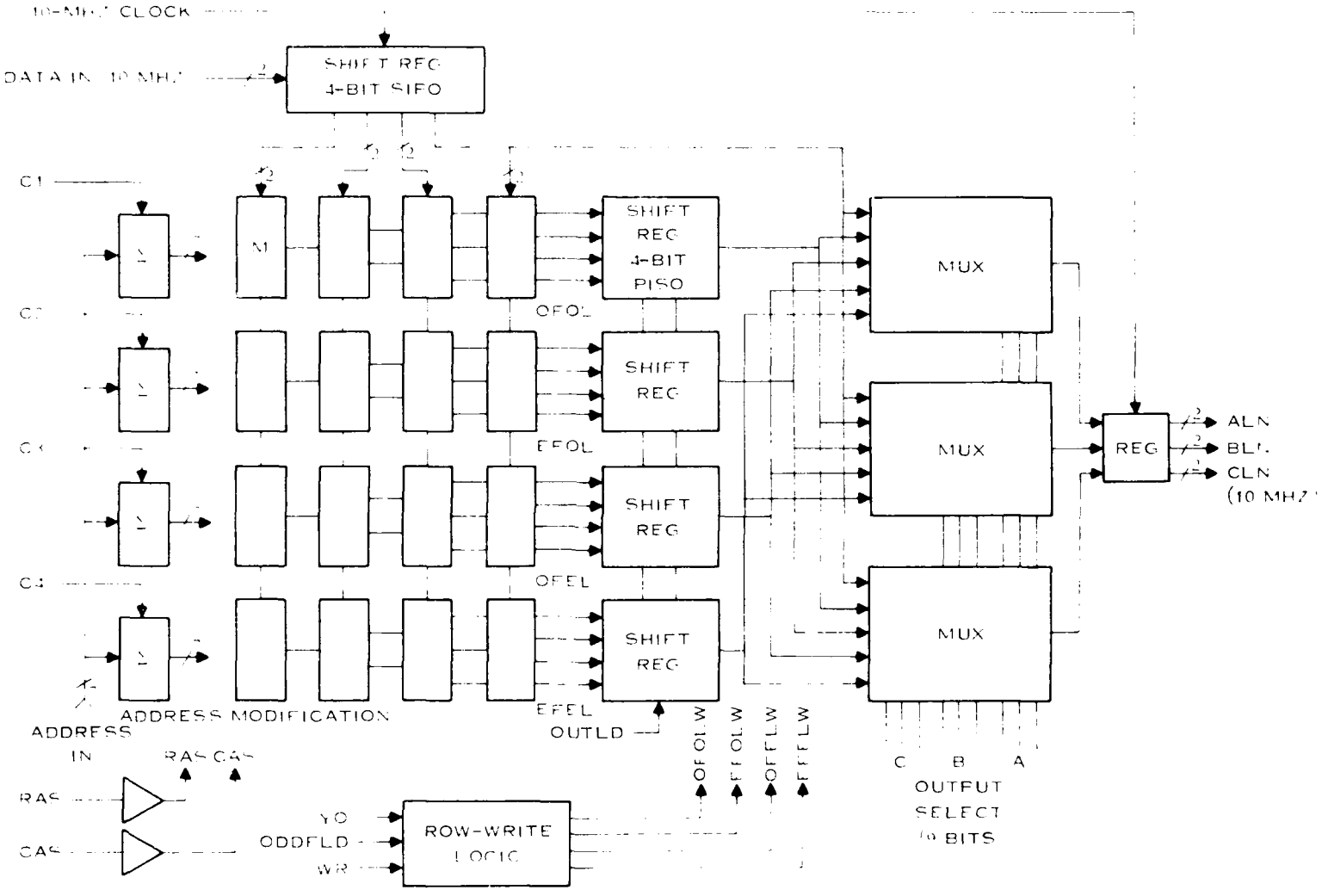


Figure 36. PIPE Demonstration Brassboard Buffer Video RAM Board

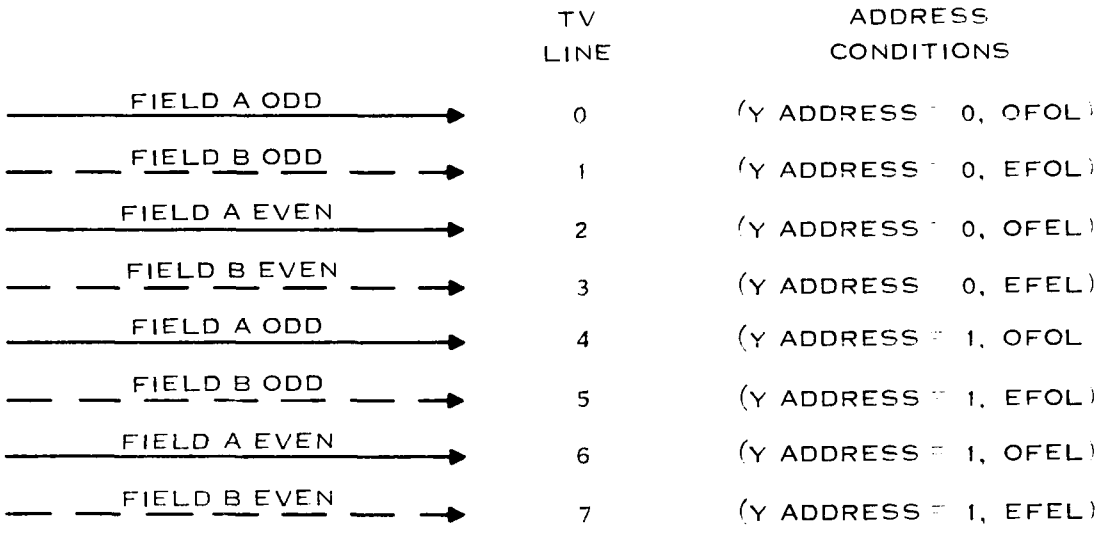


Figure 37. TV Display

difficult situation arises: the y address of the EFEL memory bank remains 0 and the y address of the OFOL and EFOL memory banks are incremented by 1 to obtain the proper y address.

High-speed adders implement modifications to the y address. Constants C1, C2, C3, and C4 are generated on the timing board and added to a base y address to create the modified y address for the memory banks.

4. PIPE LSICs and Interface

The PIPE LSIC is capable of operating on 9 × 1 or 3 × 3 blocks of data, either of which may be sliding or nonsliding. The PIPE LSIC calculates the sum of products for the nine 8-bit data words that have been loaded into the LSIC input latches by the LSIC input strobe control line. LSIC control line LOAD determines the data to be processed, and the PIPE brassboard must have circuitry to control the generation of the LOAD pulse for the various types of input data arrangements. To increase throughput, eight PIPE LSICs are used in the brassboard; all inputs of the LSICs are connected, and data is strobed into all devices simultaneously. An input controller generates the appropriate LOAD pulses to allow the eight PIPE LSICs to operate in parallel, and an output controller selects the outputs of the devices for postprocessing functions.

The eight PIPE LSICs, input controller and output controller are partitioned into two wirewrap boards (Figure 38). Each board contains four PIPE LSICs (Figure 39) and either the input or output controller. All the data inputs are connected, as are many of the other control signals—word length, 2's complement data (TCD), clock, parallel serial select, etc. Each PIPE LSIC has a separate LOAD, ENABLE, and DATA VALID control line. The 20-bit outputs of the PIPE LSICs are also connected.

Figure 38. PIPE LSIC and Interface Boards

a. Input Controller

The input controller (Figure 40) uses two 256 × 4-bit PROMs and a BCD value of the number of input strobes between LOAD pulses to generate the LOAD pulses for the PIPE LSICs. The input controller can generate LOAD pulses for seven different types of operations:

Serial operations

- 9 × 1 nonsliding, same or different weights in PIPE LSICs
- 9 × 1 sliding, same weights

Parallel operations

- 3 × 3 nonsliding, same weights
- 3 × 3 nonsliding, different weights
- 3 × 3 sliding, same weights
- 3 × 3 sliding, different weights
- 3 × 3 sliding, paired weights

The serial operations are for calculating transform coefficients and pole-zero filtering. The parallel operations are ideally suited for neighborhood operators. The arrangement of the weighting coefficients in the eight PIPE LSICs is important in determining the loading sequence of the devices. For operations with

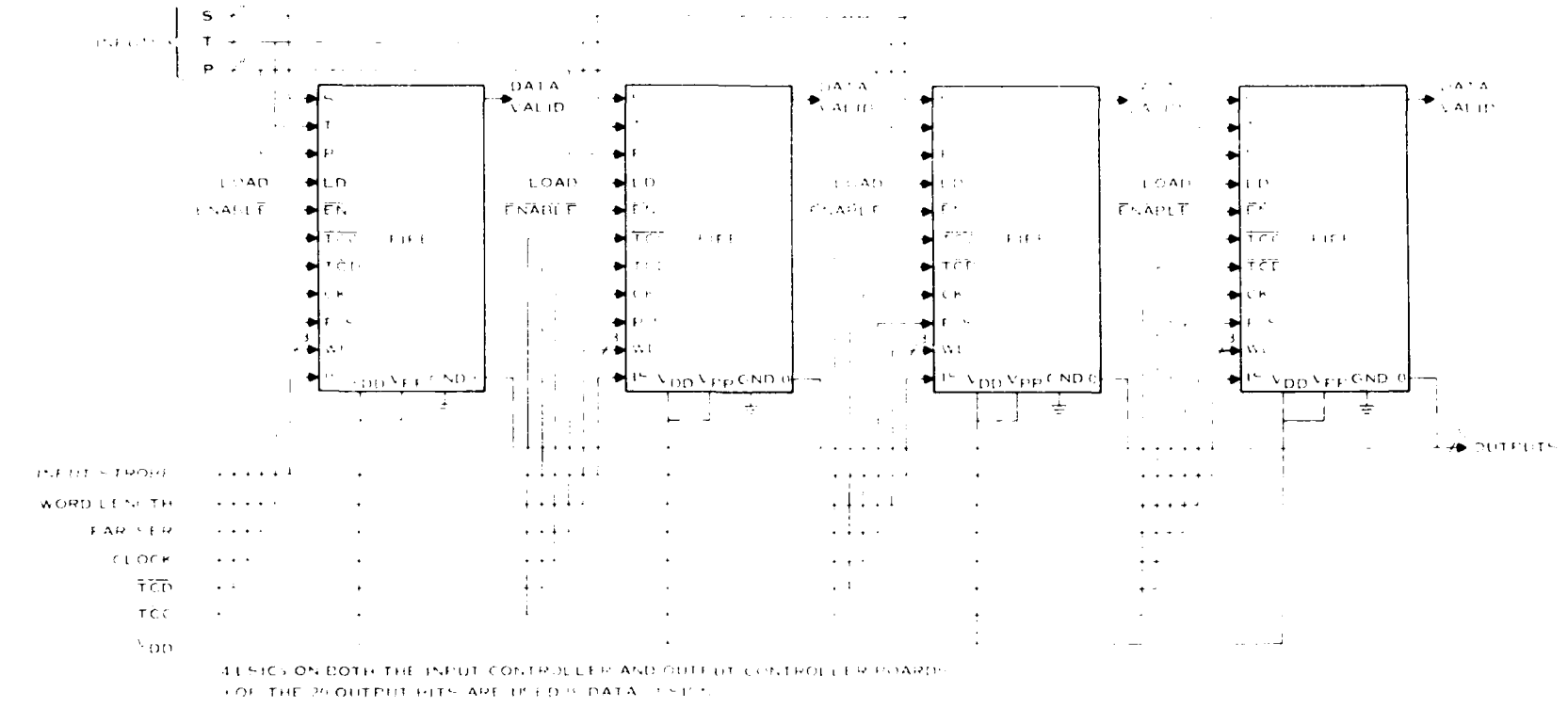


Figure 39. LSIC Module, PIPE Demonstration Brassboard

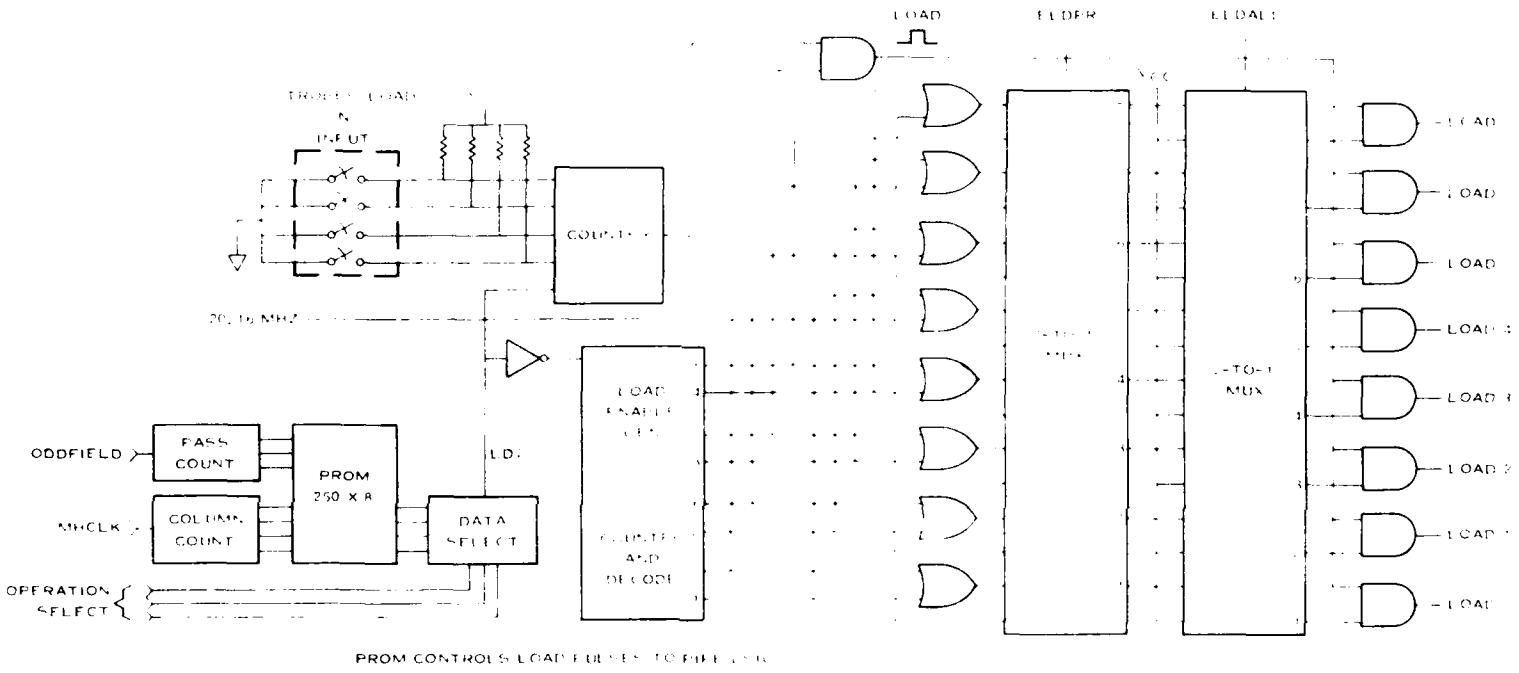


Figure 40. *LSIC* Input Controller, PIPE Demonstration Brassboard

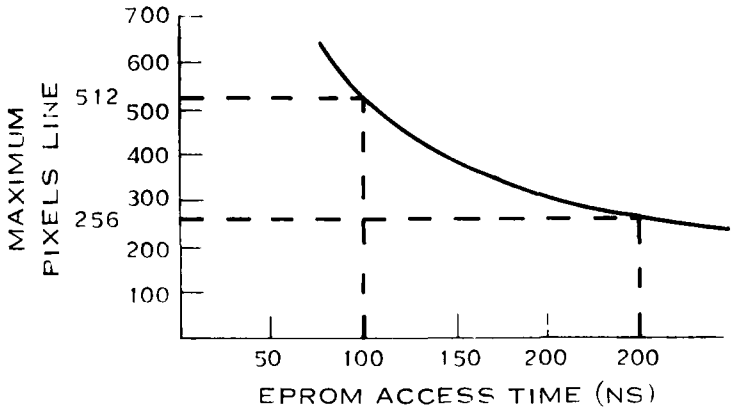


Figure 41. PIPE Demonstration Brassboard Processing at 30 Frames/Second (8-Bit Data; 3 × 3 Sliding Window; Same Weights) Image Size Versus EPROM Access Time

the same weighting coefficients in each PIPE, the throughput of the brassboard is eight times the throughput of a single PIPE LSIC because each PIPE LSIC is loaded sequentially, allowing each device to calculate an answer for adjacent neighborhoods of the image. For operations with different weights in each PIPE LSIC (template-matching edge detectors), eight PIPE LSICs are required for maximum throughput, with one template assigned to each PIPE. For differential edge detectors (Sobel, Prewitt, etc.), the weighting coefficients are arranged in pairs: the first four PIPE LSICs calculate the horizontal response; the last four calculate the vertical response.

Because of the PIPE LSIC EPROM access time and the particular requirement of certain operations, the PIPE brassboard does not process 512 × 512 images at 30 frames/second. Figure 41 indicates the effect of EPROM access time on the maximum number of pixels per line, assuming 30 frames/second. Assuming a 100-ns EPROM access time, the PIPE brassboard could process a 512 × 512 image for 3 × 3 sliding window/same weights operations at 30 frames/second. The EPROM access time is approximately 170 ns, however, as discussed in the PIPE LSIC section. Only an image size of 512 × 313 can be processed at 30 frames/second.

An alternative to reducing image size is to reduce the frame rate. Figure 42 shows the frame rate as a function of PIPE LSIC EPROM access time for the 3 × 3 sliding window/same weights and 3 × 3 sliding window/paired weights (Sobel).

To maintain the capability of the brassboard to evaluate future processors, the PIPE brassboard operates on 512 × 512 images at the frame rate dictated by the EPROM access time and the type of operation. Table 8 shows the number of passes each operation must take through a 512 × 512 image and the resulting frame rate. The input controller records the window location on a line and the number of

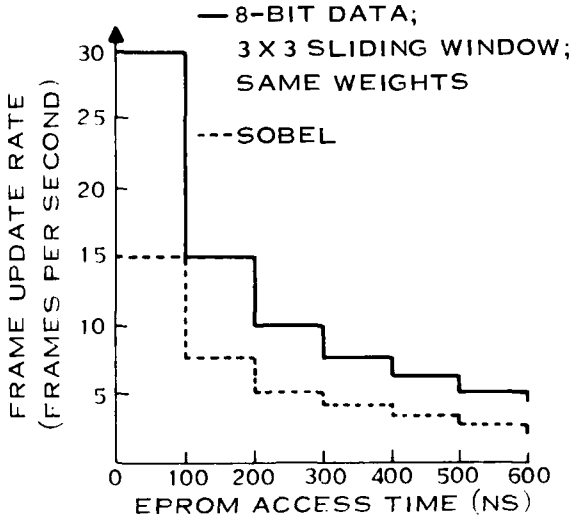


Figure 42. Frame Update Rate Versus EPROM Access Time for a 512 × 512 Image

passes made, to address the timing PROM that generates the load clock. The load enable generator and the multiplexers (Figure 40) provide different modes of input data demultiplexing to accommodate transform coefficient calculations and differential edge detectors. To calculate transform coefficients and template-matching edge detectors, all eight PIPE LSICs must be loaded with the same data; i.e., have the same load pulse. This is accomplished by enabling the second multiplexer of the input controller, thus jointly activating LOADS 0–7. For differential edge operators, the same data is needed by the first and fifth PIPE LSICs, the second and sixth, etc. This pairing of LOAD pulses is accomplished by the OR gates and first multiplexer of the input controller.

TABLE 8. FRAME RATES FOR VARIOUS OPERATIONS ON 512 × 512 IMAGE

Operation	No. of Passes	Frame Rate (fps)
9 × 1 nonsliding window; same or different weights	2	15
9 × 1 sliding window; same weights	2	15
3 × 3 nonsliding window; same weights	1	30
3 × 3 nonsliding window; different weights	6	5
3 × 3 sliding window; same weights	2	15
3 × 3 sliding window; different weights	16	1.875
3 × 3 sliding window; paired weights	4	7.5

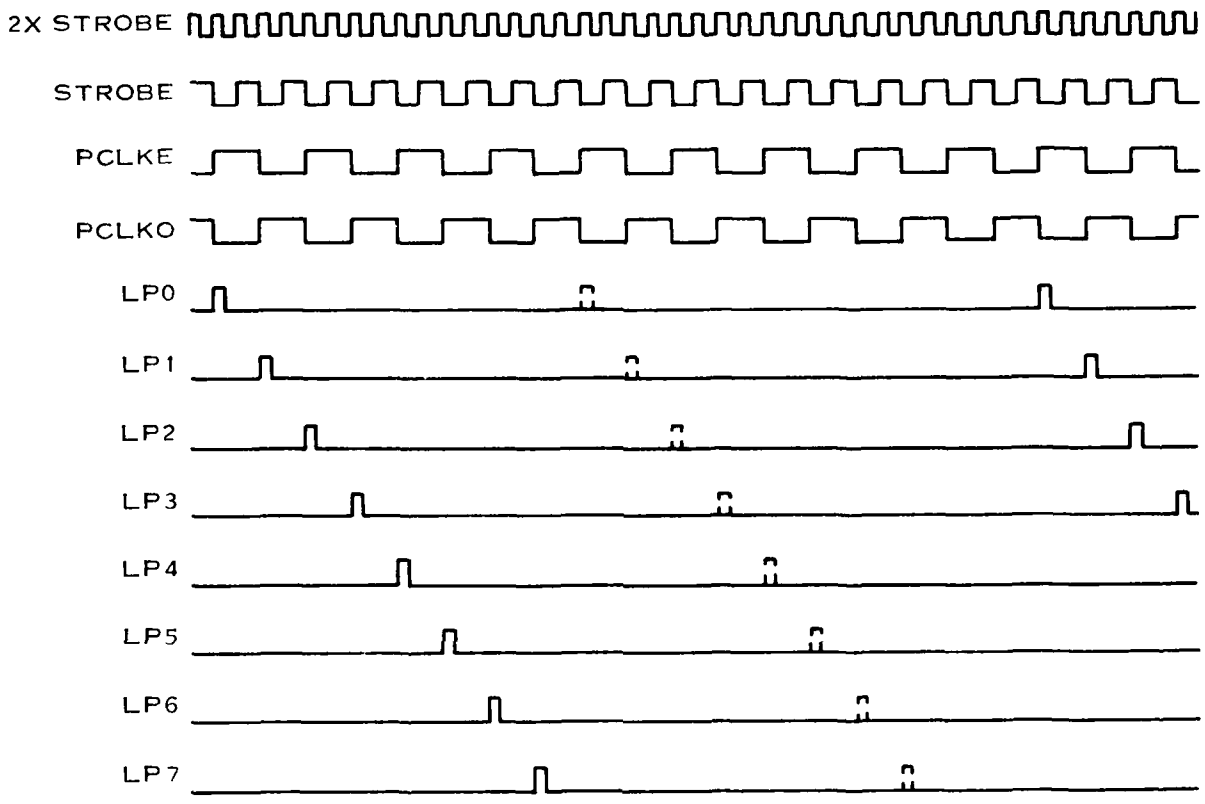


Figure 43. LSIC Input Controller Timing, 3 × 3 Sliding Window Operation (Same Weights in All PIPE LSICs)

Figures 43, 44, and 45 illustrate the LOAD pulse (LP) timing for the 3 × 3 sliding window with same, different, and paired weights, respectively. A two-phase PIPE LSIC clock, PCLKE and PCLKO, prevents certain pixels from being ignored as a result of the difference in the strobe frequency (10 MHz) and the PIPE LSIC clock rate (5 MHz).

b. Output Controller

The outputs of the eight PIPE LSICs are controlled by an output controller (Figure 46), which selects any one, any pair, or all of the outputs for postprocessing. The output controller generates the tristate enable timing for the PIPE LSICs based on the type of LSIC operation.

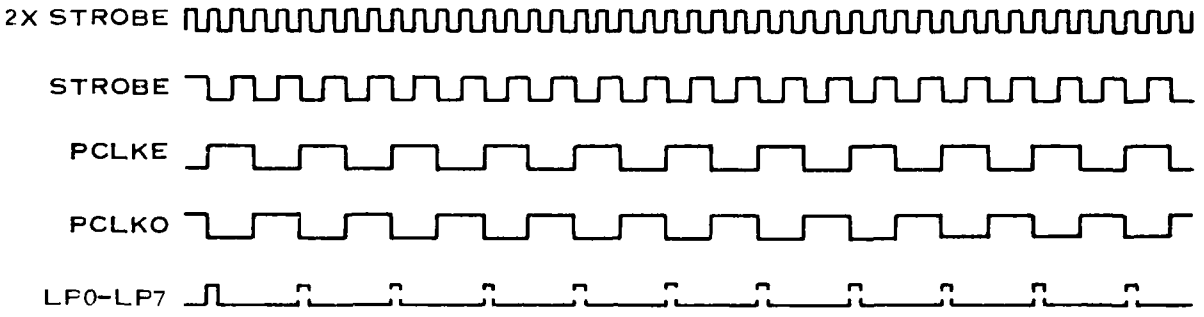


Figure 44. LSIC Input Controller Timing, 3 × 3 Sliding Window Operation (Different Weights in All PIPE LSICs)

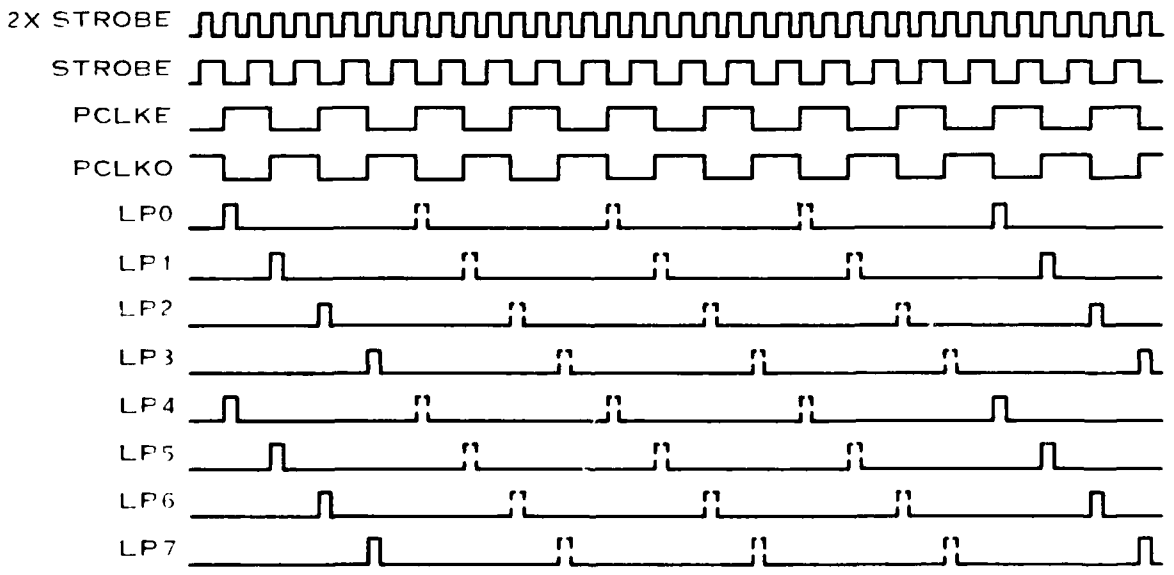


Figure 45. LSIC Input Controller Timing, 3 × 3 Sliding Window Operation (Paired Weights – Sobel)

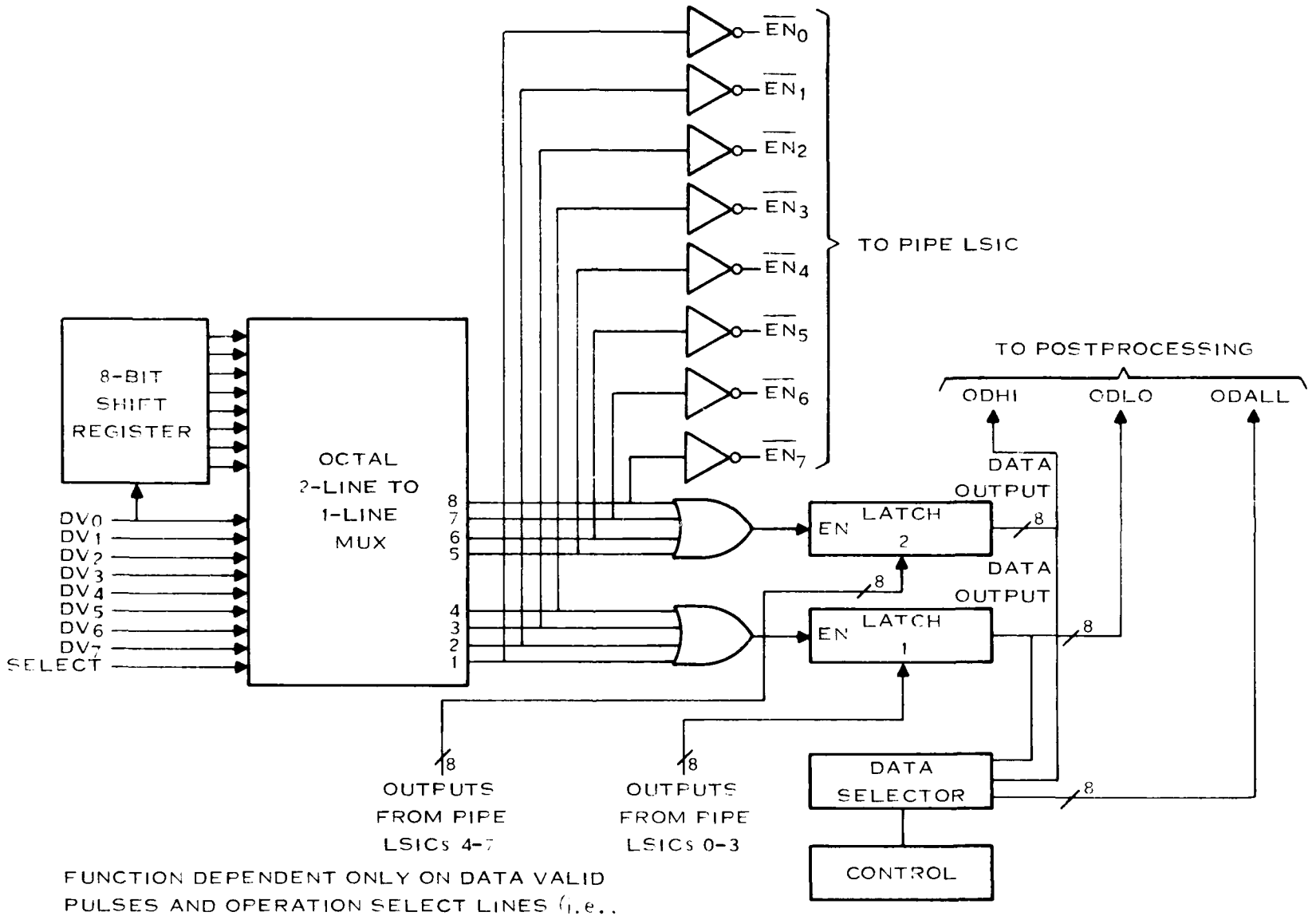


Figure 46. LSIC Output Controller PIPE Demonstration Brassboard

The DATA VALID generated by the PIPE LSIC is used to multiplex the outputs of the eight PIPE LSICs in much the same way the LOAD pulse was used to demultiplex the inputs. For operations in which the LOAD pulses are generated sequentially, the DATA VALID pulses occur sequentially and the output control multiplexer selects the DATA VALID pulses as ENABLE signals for the PIPE LSICs. For operations in which the LOAD pulses are generated in parallel, the DATA VALID pulses also occur in parallel and cannot be used to enable the PIPE LSICs because the outputs of the four PIPE LSICs on each LSIC module are connected. Therefore, the PIPE LSICs must be enabled sequentially. This is done by loading one of the DATA VALID pulses into an eight-stage serial-in parallel-out shift register; as the DATA VALID pulse is shifted down the shift register, the outputs are used to enable the PIPE LSICs sequentially.

The outputs of each set of four PIPE LSICs are loaded into 8-bit latches. (Only 8 bits of the LSIC's 20-bit output are used because the postprocessing and refresh memory functions are designed for 8-bit output values.) Rather than using the 8 LSBs of the 20-bit output of the PIPE LSICs, outputs D_7 through D_0 are utilized. This represents a divide-by-4 of the output but allows more efficient use of the dynamic range by preventing overflow (which causes saturation of the postprocessing electronics) for certain image-processing operators, notably the Sobel edge operator and fifth-level template-match edge detector. Other operators' weights can be adjusted slightly to take advantage of this increased dynamic range. Outputs D_{10} through D_8 are used to indicate overflow or underflow, and D_{19} is the sign bit.

For the 3×3 sliding window paired weights operation, two 8-bit data words (ODHI and ODLO, one from each set of the four PIPE LSICs) are presented to the postprocessing functions. For all other operations, the output controller's data selector presents a single 8-bit word (*ODALL*) to the postprocessing circuitry.

Figures 47, 48, and 49 show output controller timing for the 3×3 sliding window and same, different, and paired weights, respectively. The DATA VALID (DV) pulses and the corresponding PIPE LSIC ENABLE (EN) pulses are shown. Output data from the PIPE LSICs are loaded into latches on the falling edge of the ENABLE pulse.

5. Postprocessing

To condition the outputs of the PIPE LSICs for storage in the refresh memory and for subsequent display, a limited amount of postprocessing electronics is included in the demonstration brassboard. To calculate the magnitude of the horizontal and vertical response of the differential edge operators, a simple magnitude function, a sum of absolute values, is provided. Also included is a coarse (3 bits) direction calculation. Also provided is the ability to find the maximum of eight inputs for determining edge orientation using template-matching edge detectors.

There is also the option to bypass the postprocessing functions because postprocessing is not required in some applications. Additionally, an operator-controlled threshold is provided to permit evaluation of various thresholds on different image-processing algorithms. The operator selects a threshold

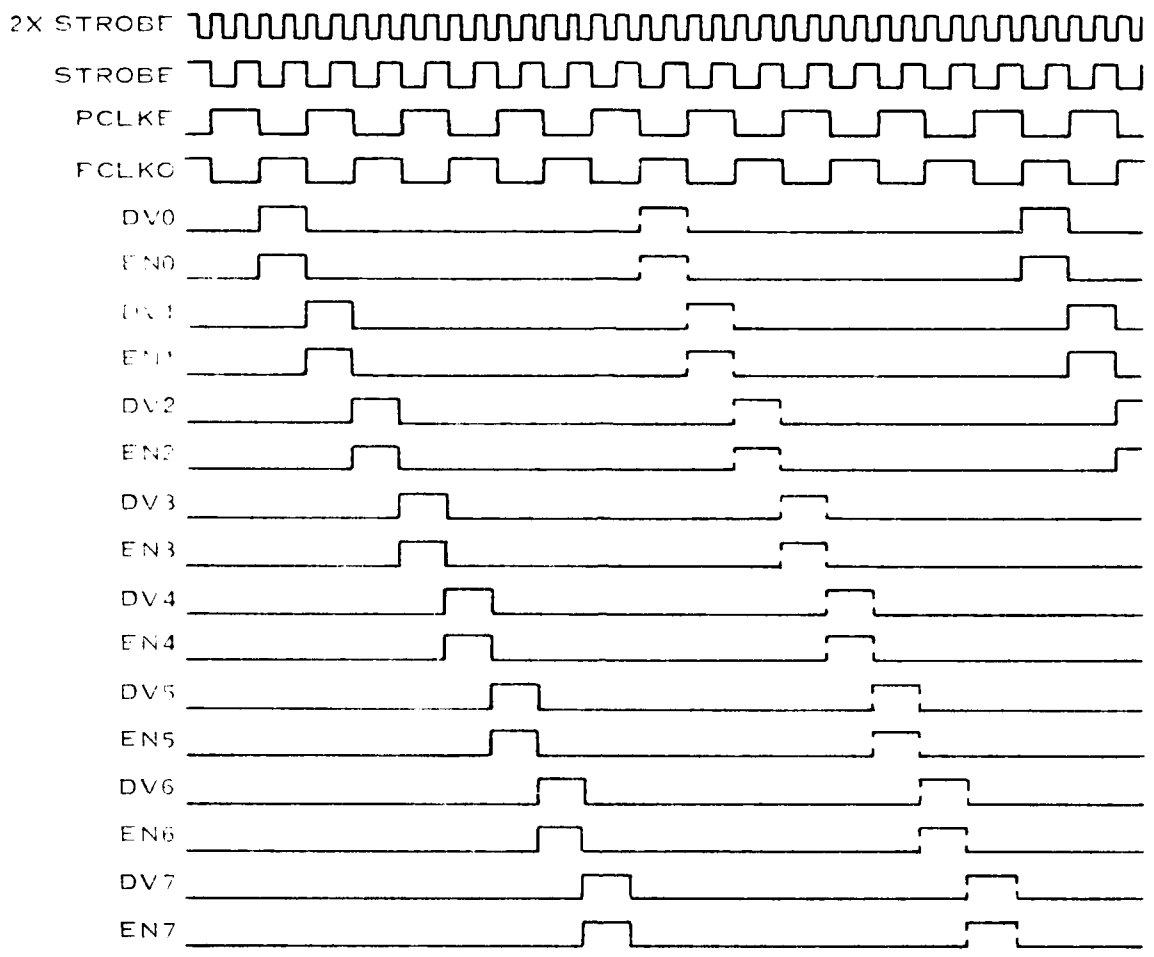


Figure 47. LSIC Output Controller Timing, 3 × 3 Sliding Window Operation (Same Weights in All PIPE LSICs)

(0–255), and decides if values above or below the threshold value are to be passed directly to the refresh memory: if values above the threshold are to be passed unmodified to the refresh memory, all data values below the threshold will be set to 0, if values below the threshold are to be passed to the refresh memory, all values above the threshold will be set to 255. The postprocessing also has circuitry to pass −255 for negative overflow conditions when the operator selects the magnitude function; when other postprocessing functions are selected, a 0 is passed for negative input values. This prevents the display of negative pixel values as positive values on the monitor.

The postprocessing board, which also contains part of the refresh memory controller circuitry, is shown in Figure 50.

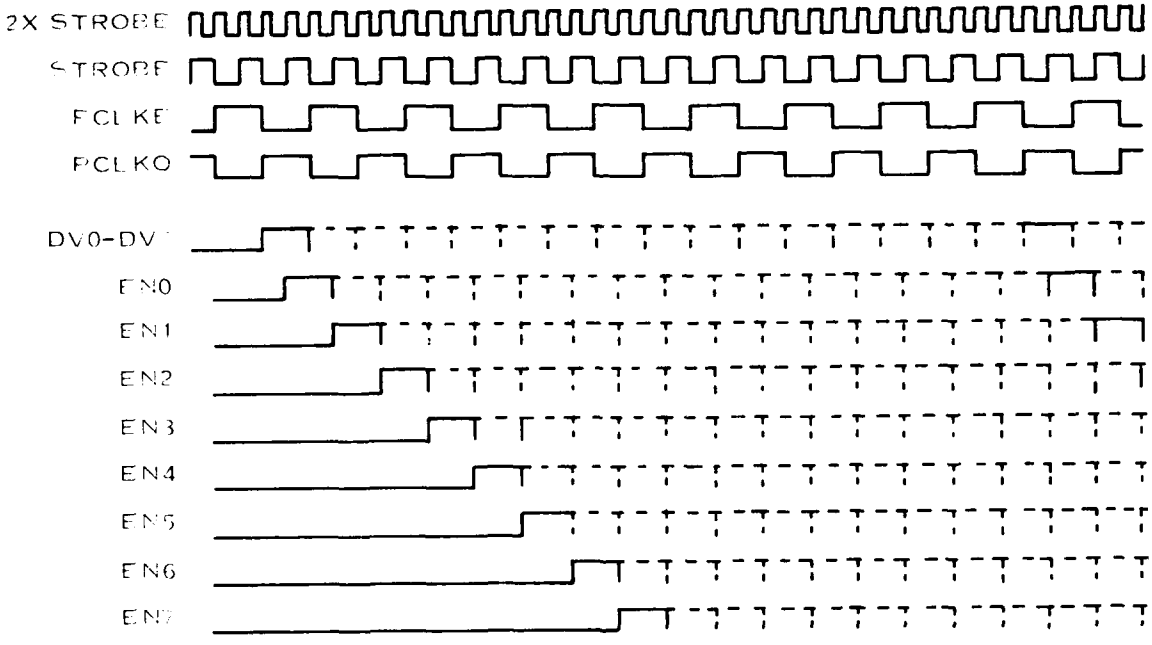


Figure 48. LSIC Output Controller Timing, 3 × 3 Sliding Window Operation
(Different Weights in Each PIPE LSIC)

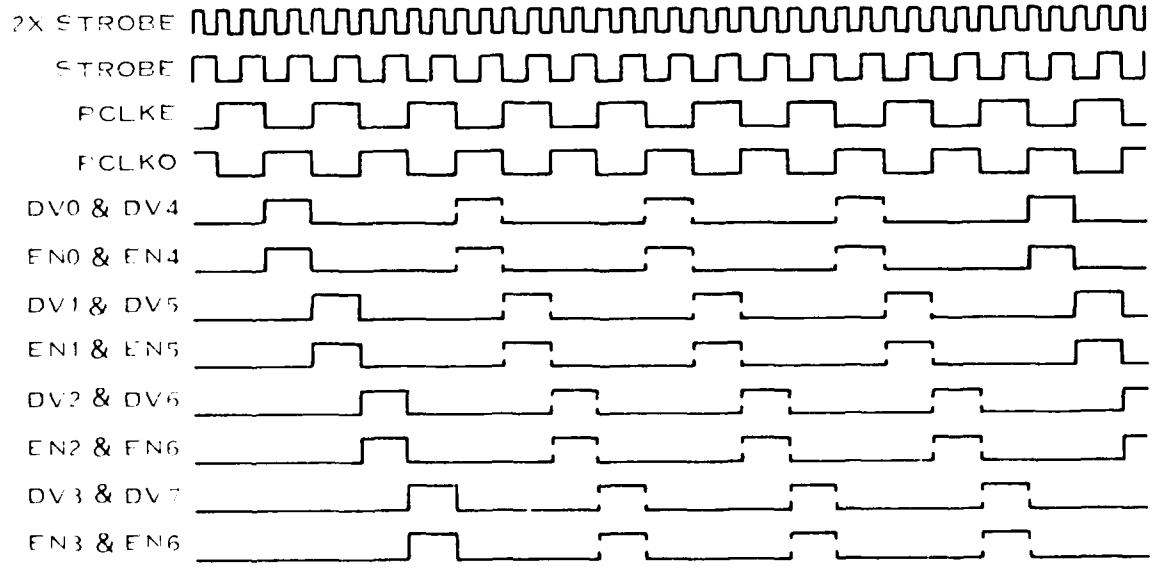


Figure 49. LSIC Output Controller Timing, 3 × 3 Sliding Window Operation
(Paired Weights - Sobel)

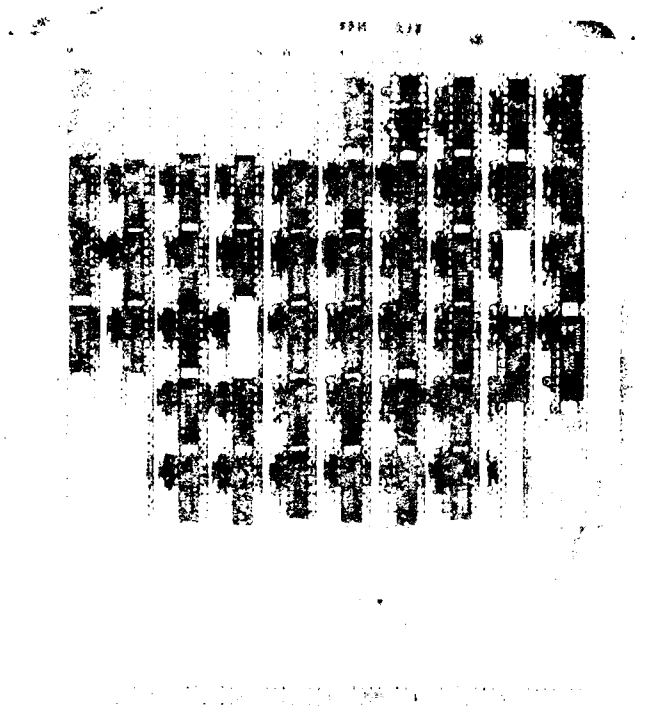


Figure 50. Postprocessing Board

In Figure 51, a simplified block diagram of the postprocessing electronics, input signals ODHI, ODLO, and ODALL represent the data from the PIPE I SIC output controller. The output select signals are decoded from the brassboard's front panel. For magnitude operations, data inputs ODHI and ODLO, which represent the outputs of each set of four PIPE I SICs, are used. For finding the maximum of eight inputs or for no operation, the data inputs ODALL, which represent the outputs of all eight PIPE I SICs, are used.

The sum-of-absolute-values function is implemented for circuitry simplicity. The absolute value of negative input values (D7 high) is formed by adding 1 to the 1's complement of the negative values. If D_7 is low, indicating a positive input value, the value is unchanged. If a positive overflow exists, the value 255 is passed. If a negative overflow exists, the value −255 is passed to the absolute-value circuitry.

A coarse 3-bit edge direction is calculated using the sign bits of the horizontal and vertical responses and knowledge of the magnitudes. V_{sign} and X_{sign} are defined as the sign bits of the horizontal and vertical response, respectively, and X_{mag} is the magnitude of the horizontal response being greater than the vertical response. Figure 52 shows the eight possible edge directions and the relationship of the sign bits and magnitudes. The logic implementation of the edge direction is straightforward and is also shown in Figure 53. The calculation of X_{mag} requires a 9-bit adder and uses the 9-bit comparison function. The

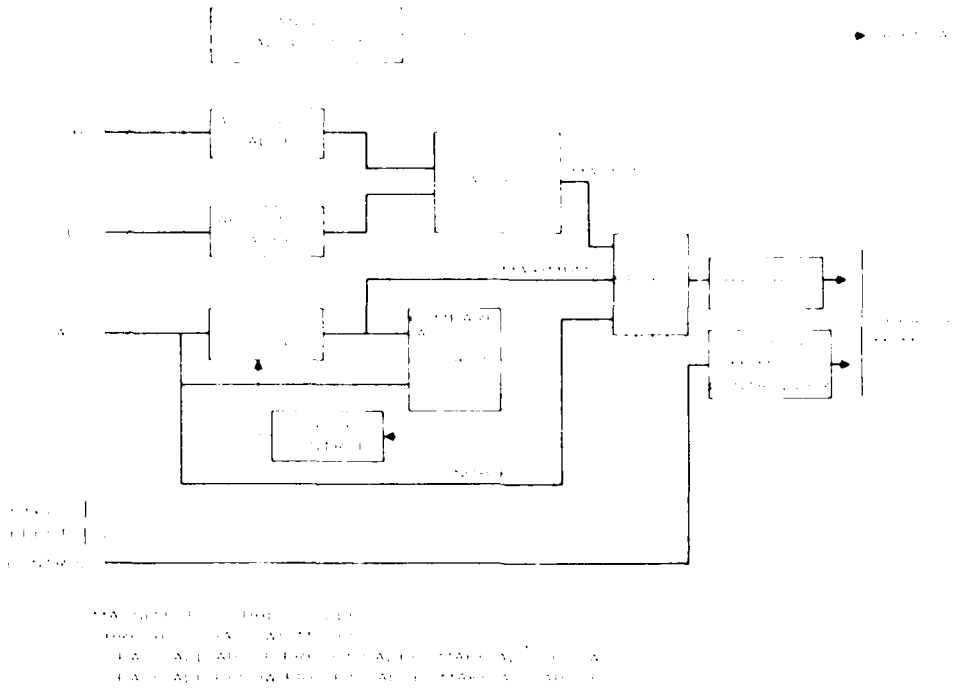


Figure 51. PIPE Demonstration Brassboard Postprocessing

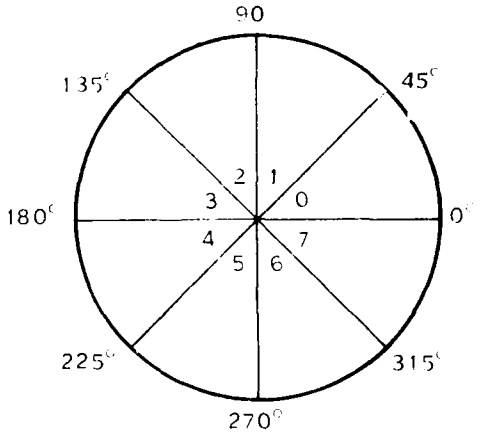
absolute-value functions already exist. The 3 output bits D_2, D_1, and D_0 represent the edge direction quantized to 45 degrees.

The maximum-of-eight input is also straightforward. The output of a PIPE LSIC is loaded into an 8-bit latch and compared to the next available LSIC output: if the most recent PIPE LSIC output is larger than the value stored in the latch, it is loaded into the latch; if it is not larger, the value in the latch is unchanged. After all eight PIPE LSIC outputs have been tested, the latch contains the maximum value. If a positive overflow condition exists, the value 255 is displayed; if a negative overflow exists, a 0 is displayed. For no-operation postprocessing, only positve values betwen 0 and 255 are displayed; negative values are replaced by 0, and values greater than 255 are replaced by 255.

The operator has complete control over the postprocessing function, selecting the function, magnitude, maximum-of-eight or no-operation processing to pass to the refresh memory.

6. Refresh Memory

The refresh memory has two functions: it accepts data from the postprocessing electronics and provides digital words to the DAC for reproducing analog video. These functions cannot be performed at the same speed and thus, must be synchronized. Implementation of the refresh memory is almost identical to that of the buffer memory, differing only slightly in the write and output sections to account for the output controller and postprocessing timing. The refresh memory stores a complete video frame (512 ×



45° ANGLE SECTORS

SECTOR	A_H	A_V	A_Z
0	0	0	1
1	0	0	0
2	1	0	0
3	1	0	1
4	1	1	1
5	1	1	0
6	0	1	0
7	0	1	1

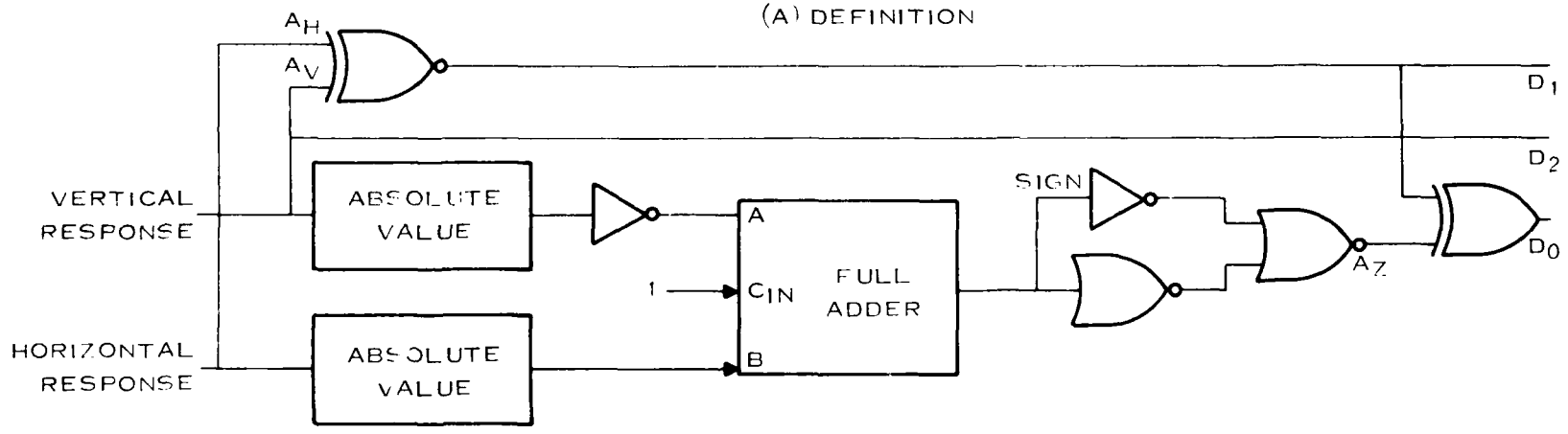
TRUTH TABLE

$A_H \triangleq$ SIGN BIT OF HORIZONTAL

$A_V \triangleq$ SIGN BIT OF VERTICAL

$A_Z \triangleq |H| \geq |V|$

(A) DEFINITION



(B) IMPLEMENTATION

Figure 52. Edge Direction Definition (Above) and Implementation (Below)

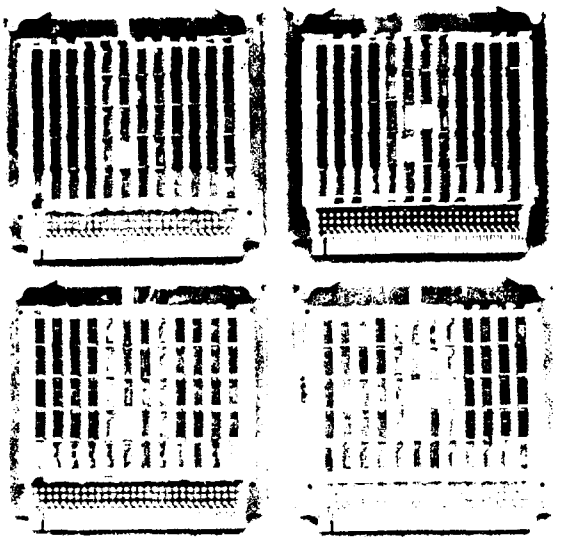


Figure 53. Refresh Memory Boards

512 × 8) and requires four wire-wrap boards as shown in Figure 53. Each board holds two bit planes, i.e., 512 × 512 × 2 bits.

Figure 54 is a block diagram of the refresh memory circuitry. As in the buffer memory, the refresh memory is partitioned into odd and even fields and odd and even lines. Also, the y address is modified using the same y address lines and address modifiers C1 through C4 as in the buffer memory. In the refresh memory, however, the x address is also modified; this is necessary to compensate for the delays in passing the data from the input to the output of the brassboard. The x address is modified by using control lines B0 through B7, which are inputs to the fast adders used for y address modification and which are also constant because the delays through the system are constant for a given operation. Another distinction versus the buffer memory is that the refresh memory does not provide the simultaneous outputs. This reduces the number of output multiplexers to one and the number of output select lines to three. The write circuitry for the refresh memory boards is also slightly different. On certain operations done by the PIPE LSICs, a single output word is produced every 16 clock cycles; therefore, two sequential PIPE LSIC outputs are not adjacent pixels on the display. This requires that each memory cell (i.e., a memory device at row x, column y in Figure 54 be written independently and exclusively of all other memory cells. Additional write enable decoding hardware provides 16 independent write pulses (WB11–WB44). Control lines Y0, ODDFLD, and WR provide a write pulse for the desired row (i.e., OFOL, OFEL, etc.) while control lines ENWB1, ENWB2, ENWB3, and ENWB4 determine which column or columns of the row receive a write pulse. Therefore, writing to any given memory cell may be done independently.

Reading data from the refresh memory is identical to the buffer memory read operation.

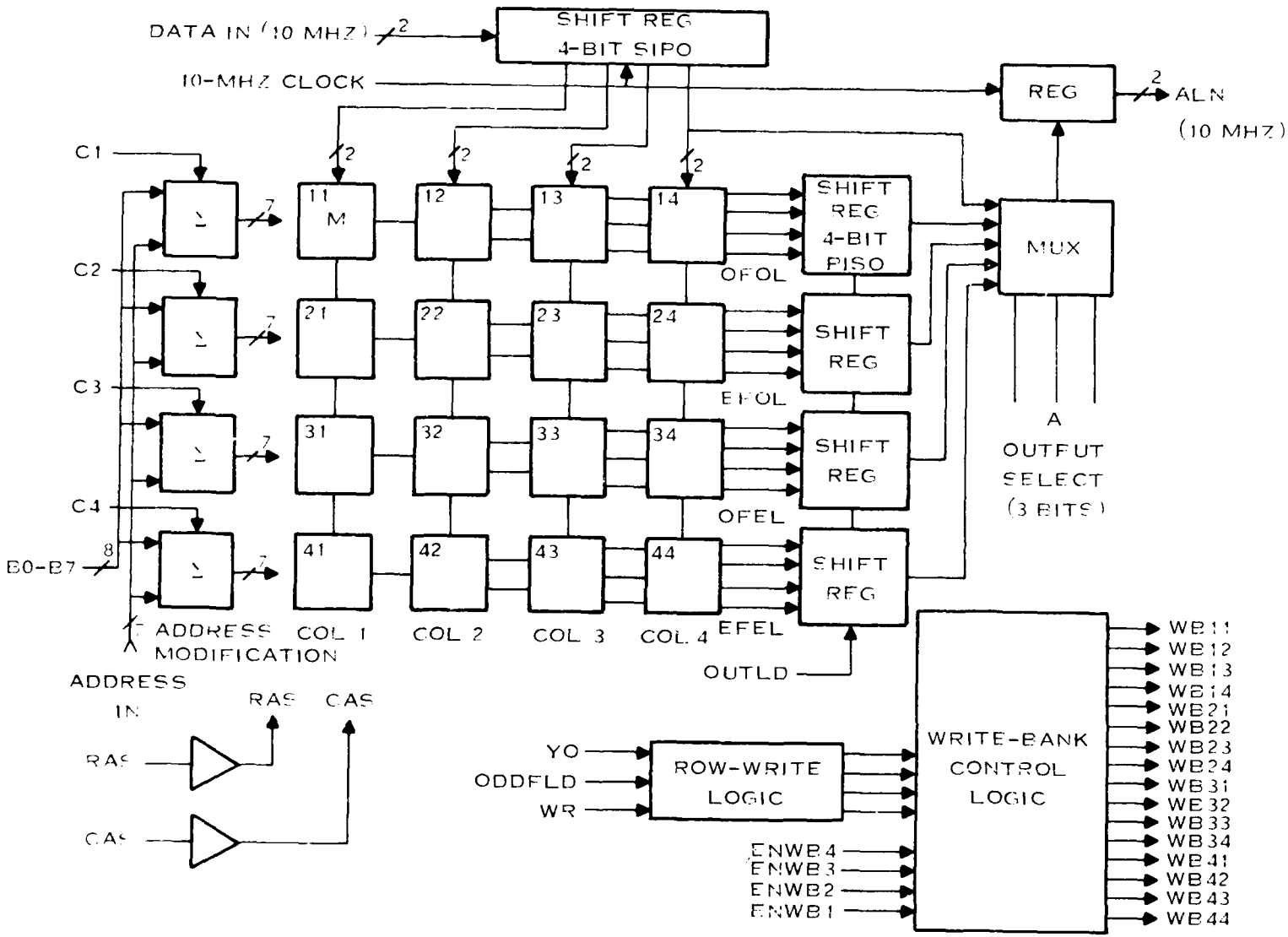


Figure 54. Refresh Video RAM Board, PIPE Demonstration Brassboard

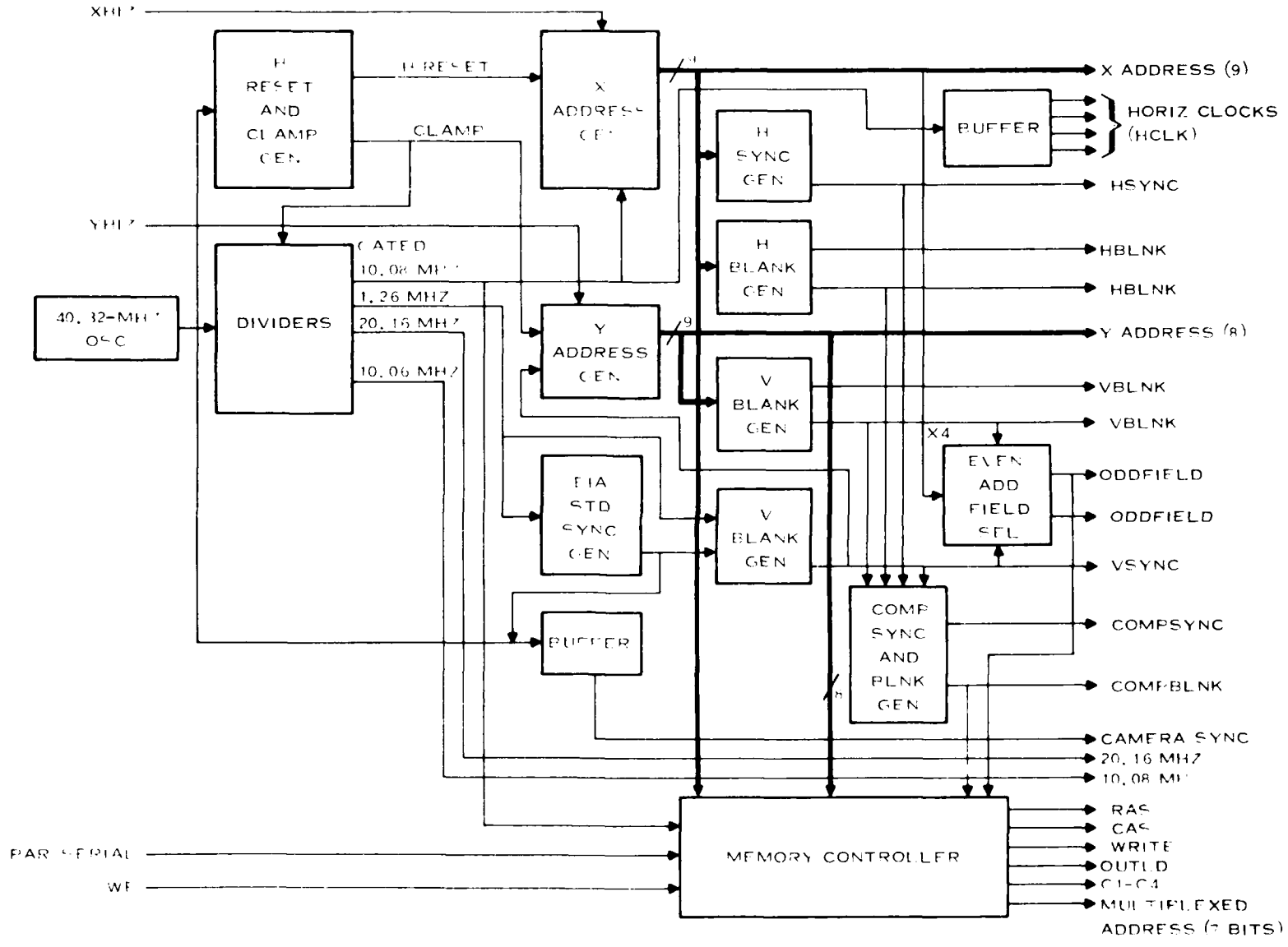


Figure 55. Timing Module, PIPE Demonstration Brassboard

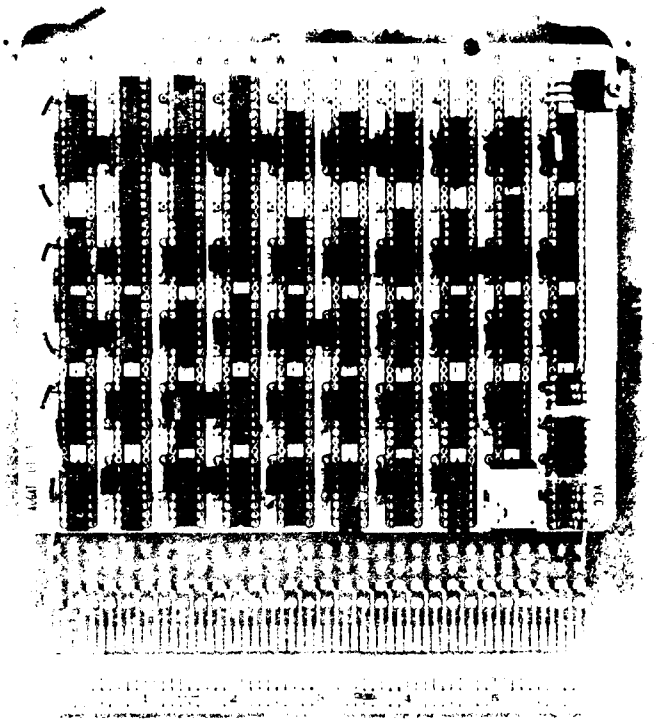
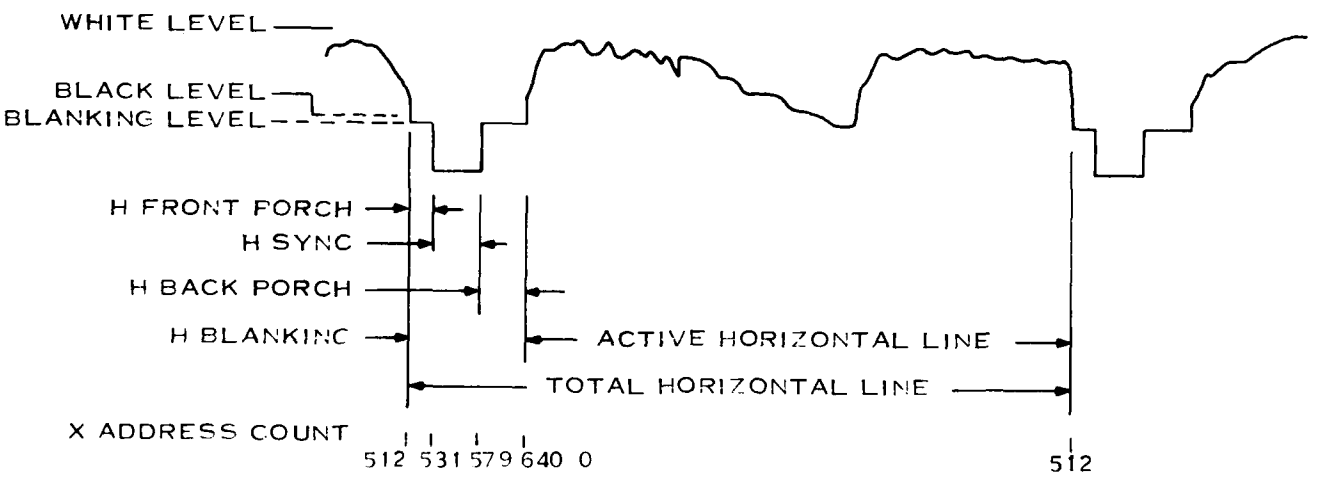


Figure 56. Synchronization and Timing Board

7. Synchronization and Timing

The PIPE demonstration brassboard contains all the synchronization and timing needed to control each of its functions. As shown in the block diagram, Figure 55, the timing board (pictured in Figure 56) generates the necessary synchronization for the COHU 4400 camera, as well as the horizontal and vertical blanking and sync and composite blanking and sync for digitizing and later creating RS–170 compatible video. The x and y addresses, row address strobe, column address strobe, write, load, and address modifiers for the buffer and refresh memories are generated on the timing board.

Camera synchronization is implemented by a commercially available TV camera sync generator IC requiring a 1.260-MHz reference. A minimum sampling time of 102.5 ns is needed to acquire 512 samples along a horizontal line of EIA Standard RS–170 video. This corresponds to a 9.75-MHz clock rate, which is not an integer multiple of the camera sync generator reference, and a slightly higher 10.08-MHz sample clock was used. The effect of this faster clock is indicated in Figure 57. For the PIPE brassboard, the active horizontal line time is 50.8 μs, a decrease of 1.7 μs from the EIA Standard RS–170 video. This minor deviation does not affect the performance of the brassboard and greatly simplifies synchronization. A 40.32-MHz crystal oscillator is used as the master clock for the brassboard to permit precise control of the various functions.



	TOTAL H LINE TIME	H BLANKING	ACTIVE H LINE TIME	H FRONT PORCH	H SYNC	H BACK PORCH
RS-170	63.5 μS	11.0 μS	52.5 μS	1.5 μS	4.75 μS	4.75 μS
PIPE BRASSBOARD	63.492 μS	12.698 μS	50.793 μS	1.885 μS	4.762 μS	6.051 μS

Figure 57. EIA Standard RS-170 and PIPE Brassboard Horizontal Timing Relationships

Horizontal, vertical, and composite blanking and synchronization are generated from the x and y addresses. The 9-bit x address is implemented with synchronous counters clocked by the gated 10.08-MHz clock. The x address counts from 0 to 511 during the active horizontal line time; during the 512 to 640 count, the horizontal blanking pulse is active, and at 640 the x address generator is cleared to 0. Correspondingly, during the 531 to 579 count, the horizontal synchronization pulse is active. The x address generator is preset to count 579 by the horizontal reset, which is generated from the standard composite sync generator IC. Figure 57 shows the x address count for the various horizontal timing relationships.

The y address generator is similar to the x address generator. The y address generator produces 8-bit addresses. The standard horizontal sync pulse generates control signal CLAMP during the horizontal back-porch interval, clocking the y address generator. The vertical sync pulse resets the y address generator to 0. Vertical blanking occurs when the ripple carry ouputs of the y address counters indicate an overflow condition. Vertical sync is implemented using up/down counters clocked by the 1.260-MHz clock; the standard composite sync IC controls the direction of count. Composite sync and composite blanking are generated by logical ORing of the horizontal and vertical sync and blanking, respectively.

The ninth bit of the y address is an even/odd field indicator. It is generated by counting the number of transitions of the fifth bit of the x address (x4) during the period beginning with vertical blanking and ending with vertical sync; this is equivalent to counting equalizing pulses of broadcast-format video. The number of transitions of x4 during a count is compared to the number of transitions during the previous count: if there are more transitions in the most recent count, it is the even field; otherwise, an odd field is indicated.

The memory controller uses the 9-bit x address, 8-bit y address, even/odd field indicator, composite blanking, gated 10.08-MHz clock, and parallel/serial control line to create the row and column address strobe, write pulses, address modifiers, and multiplexed address for the buffer and refresh memories.

The memory controller generates only a 7-bit multiplexed x and y address for the buffer and refresh memories. As four values are written into memory is parallel, the x address is reduced by 2 bits. Additional y address bits (YO and ODDFLD) are used by the memory boards to achieve full 9-bit y addressing. A write enable (WE) control line from a pushbutton on the brassboard's front panel implements a frame-freeze function by inhibiting the write pulses to the buffer and refresh memories.

8. Control Panel

All operations of the PIPE brassboard are controlled by the user at a panel (shown in Figure 58). The front panel contains a 1-line, 24-character liquid crystal display (LCD); a 16-character (0–9, A–D, *, #) key pad; and a thumbwheel switch. An 8-bit microprocessor and peripheral interface device on the brassboard controller permits the user to set up the demonstration brassboard to implement a selected algorithm. The CPU queries the user about the type of operation (parallel or serial, sliding or nonsliding), the type of input data (2's complement or magnitude), the type of memory coefficients (2's complement

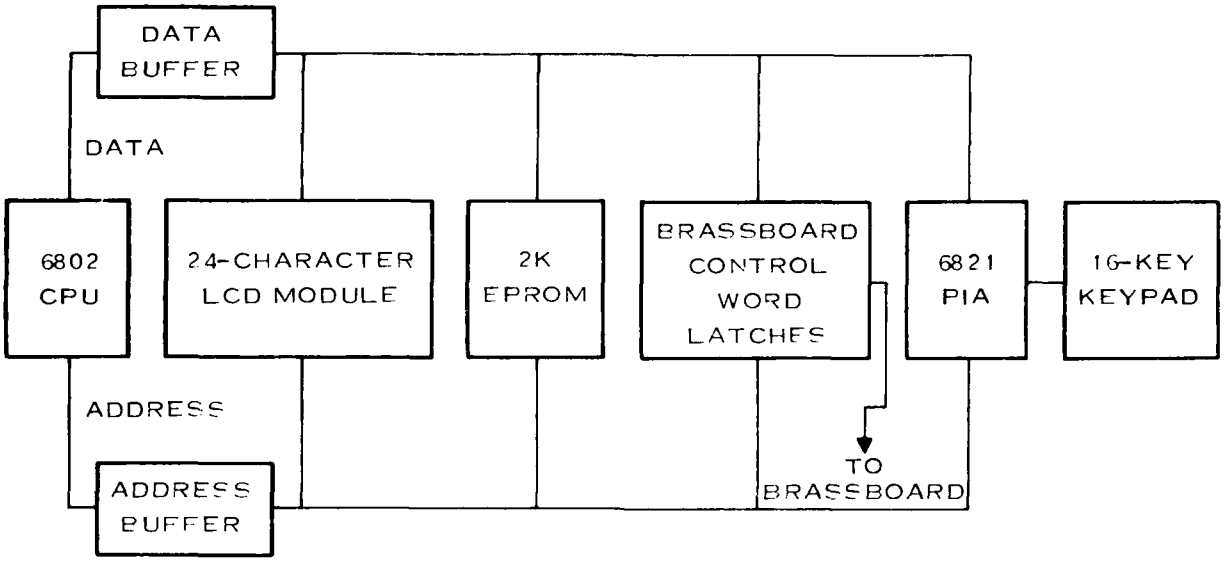


Figure 58. Front Panel Brassboard Controller

or magnitude), the length of the input word, and the type of postprocessing desired. The controller also asks how the weighting coefficients of the eight PIPE LSIC's are arranged; i.e., same weights in all the LSIC's, different weights in each LSIC, or paired weights. The controller notifies the operator if a nonvalid response has been entered; for example, a letter input when a number is required. If the operator requests an undefined operation, the controller notifies the user. On request (# key), the controller displays the current operating parameters. The * key is used to begin the process of setting up new operating parameters. The software required for the CPU is stored in a 2K × 8 EPROM and can be easily changed to upgrade or modify the operations of the brassboard.

The thumbwheel switch on the front panel is used to threshold the output and has two modes of operation to enhance the output image; either the output values above the threshold are set to gray-level 255 or the values below the threshold are set to gray-level 0.

On the key pad, symbols A, B, C, and D automatically instruct the brassboard to perform certain predefined operations. The A key represents Sobel operation: sliding, parallel, 8-bit magnitude input data; 2's complement weighting coefficients arranged in pairs; and magnitude postprocessing. When power is initially applied to the brassboard, the controller defaults to Sobel operation. The B key represents operations requiring sliding, parallel, 8-bit magnitude input data; 2's complement weighting coefficients; different weights for each PIPE LSIC; and maximum-of-eight output postprocessing. This operation is used for template-matching algorithms (i.e., compass gradient, Kirsch, etc.). Operations selected by the C key are similar to B-key operations except that the same weights are in each PIPE LSIC and a "no-op" postprocessing function is selected; this allows a sliding 3 × 3 filter to be implemented at the maximum frame rate. The only difference between C-key and D-key operations is that the latter selects nonsliding operations, allowing processing on 3 × 3 contiguous blocks of pixels.

The brassboard controller is implemented on a board located in the left rear quarter of the brassboard and connected to the front panel and other brassboard functions through 40-pin ribbon cable.

9. Summary

The main design goals of the PIPE demonstration brassboard were the ability to fully evaluate the PIPE LSIC and the flexibility to evaluate future image-processing hardware developments. Those goals have been achieved by functionally partitioning the brassboard into four major sections:

- Analog-to-Digital Conversion

  This half-board digitizes standard RS–170 video from a COHU 4400 camera into 8-bit digital data.

- Memory

  Eight boards of the brassboard are used to implement a frame buffer and refresh memory. Both memories store a complete video frame (512 × 512 × 8 bits) and are designed with 16K × 1 dynamic RAMs. Each board holds two bit planes (i.e., 512 × 512 × 2 bits).

- PIPE LSIC and Postprocessing

  These three boards contain eight PIPE LSIC's, their input and output control circuitry, and the postprocessing functions. These boards can be replaced by future processor boards and evaluated using real-time video.

- Digital-to-Analog Conversion

  This half-board converts the digital data from the refresh memory into analog data and provides the necessary synchronization to create RS–170-compatible composite video for the TV monitor.

The partitioning of the system is shown in Figure 59. A synchronization and timing board to generate the necessary clocks to control each of the brassboard functions makes the brassboard

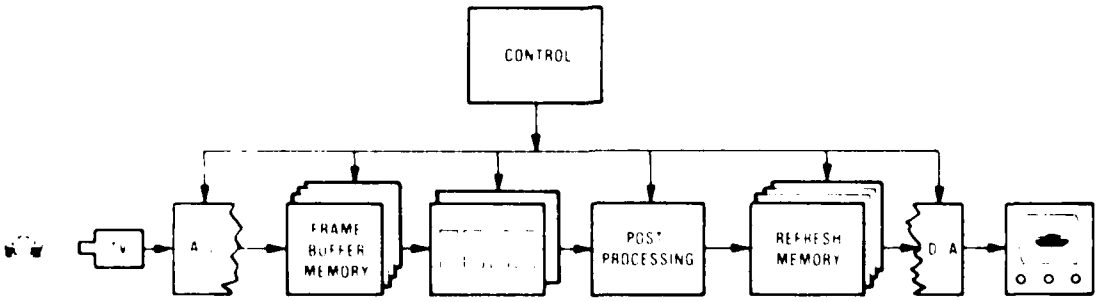
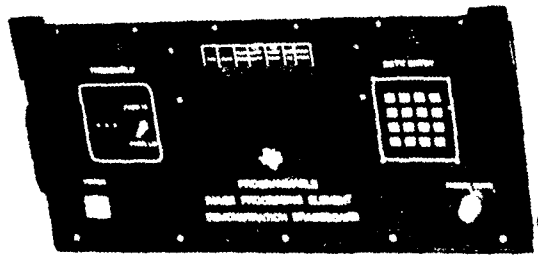


Figure 59. PIPE Demonstration Brassboard



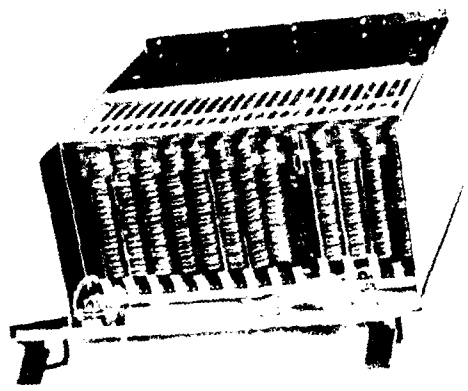


Figure 60. PIPF Demonstration Brassboard Hardware

TABLE 9. POWER AND SIZE OF PIPE DEMONSTRATION BRASSBOARD

Function	Size (in.²)	Power (W)	No. of Boards
ADC/DAC	36	14.1	1
Buffer memory	144	18.6	4
PIPE LSICs IC interface	72	15.3	2
Postprocessing	36	9.4	1
Refresh memory	144	20.3	4
Timing and control	36	6.9	1
Front-panel controller*	28	2.0	1
Total	496	86.6	14

*The front panel controller board is external to the rack assembly.

completely self-contained. To communicate the type of desired operations, an interface between the user and the PIPE LSICs is implemented through a front-panel controller.

The brassboard hardware is shown in Figure 60. The lower photograph shows the brassboard with the front panel lowered, exposing the 13 wire-wrap boards on which the brassboard's functions are constructed.

The power and size of the demonstration brassboard are indicated in Table 9. The memory function has the largest power and size requirement, but its inclusion gives the desired flexibility.

The brassboard is designed to operate in real time, i.e., thirty 512 × 512 × 8-bit video frames/s. The ADC, buffer memory, postprocessing, refresh memory, timing functions, and DAC are capable of operating with a 100-ns clock. The access time of the EPROM on the PIPE LSICs prohibits operating faster than approximately 200 ns, and multiple passes through an image are required to process an entire frame. In Table 10 are the frame rates for the various operations. These reduced frame rates are for the PIPE LSICs only and do not prohibit real-time evaluation of future processor developments.

TABLE 10. FRAME RATE FOR VARIOUS OPERATING CHARACTERISTICS

Input Data	Operation Weights	Sliding			Nonsliding		
		Same	Different	Paired	Same	Different	Paired
Parallel		15	1.875	7.5	30	5	×
Serial		15	×	×	5	15	×

× = Operations not defined.

ORIGINAL

LOW PASS FILTER OUTPUT

$$\frac{1}{1075}\begin{bmatrix} 67 & 138 & 67 \\ 138 & 255 & 138 \\ 67 & 138 & 138 \end{bmatrix}$$

Figure 61. Implementation of Low-Pass Filter

D. BRASSBOARD DEMONSTRATION

A major objective of the brassboard is to demonstrate the versatility of the PIPE LSIC. To demonstrate the PIPE LSIC capability to perform vector or transform operation requires a serial data path into the PIPE LSIC and the necessary processing of the PIPE LSIC output for display on the TV monitor. These operations are supported by the brassboard, but, because of the serial nature of the data, the display does not provide the observer an interesting image. A more meaningful demonstration of the brassboard is the parallel mode of operation. These operations show the flexibility of both the brassboard and PIPE LSIC. Neighborhood operators were used during the hardware evaluation and to demonstrate the brassboard.

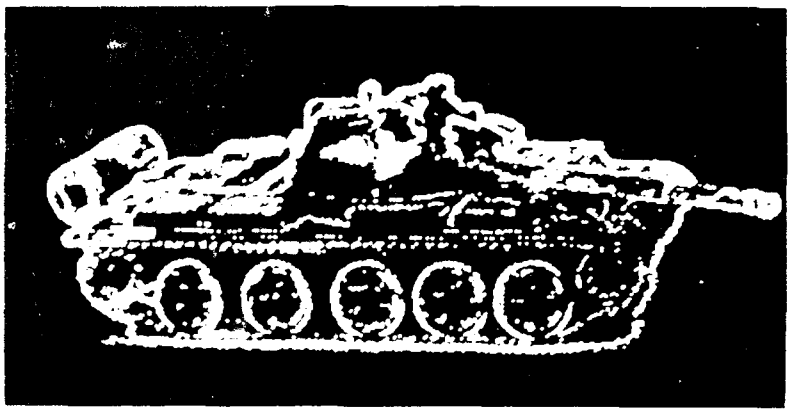
The testing of the various functions of the brassboard utilized a 3×3 sliding same-weight data in all eight PIPE LSICs, no postprocessing operation with unity operator; all 0's in the 3×3 window except for a value of 4 in the center pixel location. Recall that the PIPE LSIC outputs are shifted by 2 bits; thus, a value of 4 rather than 1 is placed in the center pixel location. With the unity operator, the output of the brassboard should be a replica of the input; any noise, ghosting, or other artifacts are readily observed.

After all the brassboard functions were operational, the weighting arrays in the PIPE LSICs were changed to demonstrate more interesting image-processing operations. A common and important image-processing operator is low-pass filtering. Several weighting arrays are suitable for low-pass filtering, but basically they all calculate the mean of the intensity levels in a small neighborhood of pixels. Figure 61 demonstrates the use of the PIPE LSICs to implement a low-pass filter. The weighting array was programmed into all eight PIPE LSICs, allowing maximum throughput. The no-postprocessing function was used. As previously discussed, the PIPE LSIC EPROM has an access time of approximately 200 ns, requiring two passes through the image; this represents a 15-Hz frame rate. Considerable blurring of the image, indicative of low-pass filtering, can be observed.

Another important image-processing operator is the edge detector. The two most common types are differential edge detectors and template-match edge detectors. Differential edge detectors require spatial convolutions of the input image with both horizontal and vertical weighting arrays. The outputs of the two convolutions are combined to produce an edge magnitude. Figure 62 shows the result of implementing the Sobel differential edge detector with a sum of absolute values as the magnitude technique. To improve throughput, four PIPE LSICs calculate the horizontal response while the other four calculate the vertical response. The magnitude postprocessing function is used. This corresponds to a 3×3 sliding paired-weights magnitude function. Only four PIPE LSICs are operating in parallel on one direction and the throughput for the Sobel operation is 7.5 frames second for $512 \times 512 \times 8$-bit images.

In template-matching edge detection, a set of weighting arrays corresponding to the eight major compass directions (north, northeast, east, etc.) is convolved with the input image. The PIPE brassboard easily implements template-matching edge detection by using each PIPE LSIC to calculate the response

ORiCINAL



SOBEL EDGE OUTPUT

VERTICAL

1	0	-1
2	0	-2
1	0	-1

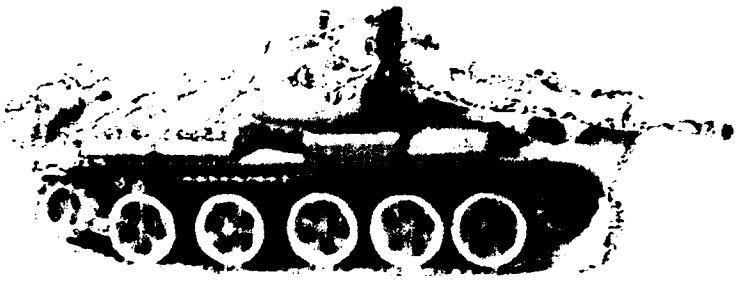
HORIZONTAL

-1	-2	-1
0	0	0
1	2	1

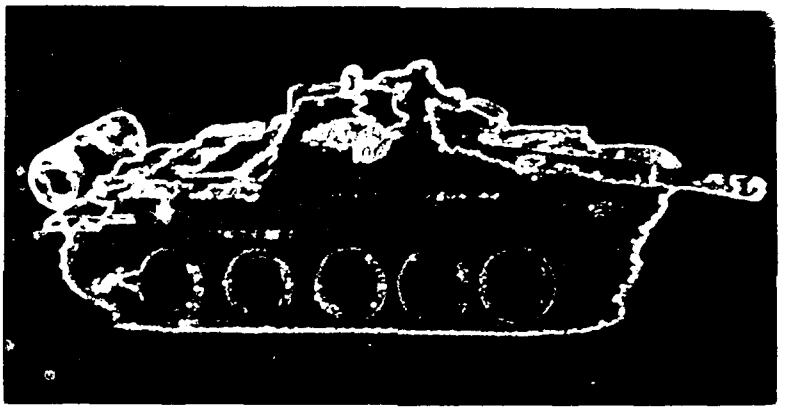
WEIGHTING ARRAYS

Figure 62. PIPE Demonstration Brassboard Implementing a Sobel Edge Detector

for one compass direction. For eight compass directions, the eight PIPE LSIC's cannot operate in parallel on one direction; therefore, the throughput for template-match edge detection is 1.875 frames/s. The maximum-of-eight postprocessing function is utilized. Figure 63 shows the PIPE brassboard implementing the fifth-level template-match edge detector. The south and west weighting arrays of the fifth-level template-matching edge detector are identical to the weighting arrays used to calculate the Sobel edges. The addition of extra weighting arrays makes the response of the template-match edge detector more exact than the response of the sum of absolute values used in the Sobel edge detector. The edge responses shown in Figures 62 and 63 are similar, but the template-match response is stronger than the Sobel response.



ORIGINAL



FIFTH-LEVEL TEMPLATE MATCH EDGE DETECTOR OUTPUT

1	2	1
0	0	0
-1	-2	-1

NORTH

0	1	2
-1	0	1
-2	-1	0

NORTHEAST

-1	0	1
-2	0	2
-1	0	1

EAST

-2	-1	0
-1	0	1
0	1	2

SOUTHEAST

-1	-2	-1
0	0	0
1	2	1

SOUTH

0	-1	-2
1	0	-1
2	1	0

SOUTHWEST

1	0	-1
2	0	-2
1	0	-1

WEST

2	1	0
1	0	-1
0	-1	-2

NORTHWEST

WEIGHTING ARRAYS

Figure 63. PIPE Demonstration Brassboard Implementing the Fifth-Level Template-Match Edge Detector

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